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(54) Image forming apparatus

Bilderzeugungsgerät

Appareil de formation d'image

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(56) References cited:
EP-A- 0 465 093
US-A- 5 229 866
US-A- 5 519 499

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Description

[0001] This invention relates to an image forming apparatus, such as a digital copying machine.

[0002] Recently, image information has come to be handled easily in the form of digital data. One of apparatuses using such technology is a digital PPC. Unlike a conventional analog PPC, it does not direct the reflected light from the manuscript optically to form an image on a photosensitive material. After the reflected light from the manuscript has been read by a CCD sensor in the form of an electric signal, it is converted into a digital signal. The digitized manuscript undergoes various processes and then is printed out on paper with a laser printer.

[0003] In US 5,229,866 an image processing system for reducing wait time before image data transfer to an image output section is described. In the system image data, as read by an image read section, is compressed and stored into a large capacity memory, the image data is read out of the memory and decompressed into the original image data, and decompressed data is output to an image output section.

[0004] The system comprises data compressing means for compressing image data, data decompressing means for decompressing the compressed image data into the original image data, data storage means of large memory capacity for storing data, a page buffer for storing the image data to be transferred to and from the data storage means, and control means.

[0005] The control means are provided for controlling the compression and expansion of the image data, and the transfer of the image data to and from the data storage means, when the image data is transferred from the data storage means to the image output section every page, the control means reading in advance the image data of two pages from the data storage means, loading the image data into the page buffer, reading the image data from the page buffer, and outputting the image data to the image output section through the page buffer.

[0006] In EP 0 465 093 A2 a method and an apparatus for stream printing in an electronic reprographic device are described. The apparatus comprises means for scanning a set of original documents, means for converting the scanning documents to electronic signals, means for storing said electronic signals for print generation, means for printing, and means for automatically determining the optimum time to commence operation of the printing means in order to allow the printing to begin prior to the completion of the scanning of all documents.

[0007] In a specific embodiment the apparatus comprises a main memory with plural hard disks for storing image data. The electronic signals are compressed to image data which are then stored into the main memory. In order to print reproduction of the documents, the image data are read out of the main memory, are decompressed, and are sent to the printer.

[0008] In US 5, 519,499, published on 21.05.1996, an image processing apparatus is described which forms an image on a recording sheet on the basis of image data obtained from image output means. The apparatus comprises temporary storage means for temporarily storing the image data input through the image input means, accumulation means for accumulating and storing the image data stored in the temporary storage means, and calculation means for calculating a period which is required for reading out image data to be processed from the accumulation means.

[0009] In a specific embodiment the apparatus comprises a compressor for compressing image data which have been read by the image input means. The output side of the compressor is connected to a buffer memory. The compressor continuously compresses data which are input from the image input means. The data output rate of the compressor is not constant. The output is transferred to the buffer memory. Every time when the transferring of compressed data of one page of documents from the compressor to the buffer memory is completed, the writing of the data from the buffer memory to a hard disk is performed.

[0010] Converting the manuscript image into a digital signal enables various signal processes, including the correction of the input characteristic of the CCD sensor or the output characteristic of the laser printer, image enlargement and reduction, partial erasure, and frame outside erasure,

[0011] Furthermore, the coding process of the image converted into a digital signal makes it possible to compress the amount of data and store it efficiently. The stored images can be decoded into the original images in arbitrary order in which the images are to be printed out, and any number of them can be printed out on the laser printer.

[0012] Since such rearrangement has been made mechanically on the copied print output (the image-copied sheets of paper) by the use of a sorter or a stacker, it is impossible to avoid a trend for the apparatus to get increasingly large and an increase in noise. In addition, printing on sheets of paper requires the copying operation repeatedly.

[0013] The time required to encode an image differs with the nature of the image and is not constant. If a scanner (CDD sensor) reads an image at a constant speed, the process cannot keep up with the reading speed and will lose part of the read-out data unless the coding process speed is sufficiently faster than the reading speed. To avoid this problem, a page of image memory is provided and a page of image data is temporarily entered from the scanner into the image memory. Thereafter, the coding process is performed on the image on the image memory. By doing so, the difference between the reading speed of the scanner and the speed of the coding process can be absorbed.

[0014] During the coding process, however, because the scanner cannot enter the image input into the page

memory, it has to wait to enter the next image input until the coding process has ended. To eliminate the waiting, two pages of image memory are provided, which enables the scanner to enter the image input into the other empty image memory even if one image memory is in the coding process. Thus, use of two pages of image memory enables the coding process and the image input from the scanner to be performed at the same time. By doing this alternately, it is possible to carry out the coding process consecutively without causing the scanner to wait to enter the input.

[0015] Furthermore, when the coded image is decoded and the decoded data is outputted to a laser printer, the process can be performed consecutively in a similar manner. Two pages of image memory are provided. At the same time that the decoded image is written into one image memory, the already decoded image in the other image memory is read out and outputted to the laser printer. By doing this alternately, it is possible to perform the process consecutively without causing the laser printer to wait to output images.

[0016] The above-described consecutive process requires two pages of image memory. To copy a manuscript with a high picture quality, it is necessary to raise the resolution at which the manuscript is read or images are printed on the laser printer.

[0017] Naturally, as the resolution gets higher, the capacity of image memory required to achieve the resolution grows enormous. For example, when a page of A4-size manuscripts is read at a resolution of 400 dpias monochrome data with one bit per pixel, the capacity of image memory needed is about 2 Mbytes; and when the same page is read at a resolution of 600 dpi, the image memory capacity needed is about 4.4 Mbytes. Furthermore, when the same page is read as gray scale data with 8 bits per pixel, the image memory capacity needed is as enormous as eight times the above memory capacity.

[0018] As described above, to record image data requires a tremendous capacity of memory. If two pages of memory are necessary, it will be impossible to avoid problems including an increase in costs, an increase in the number of component parts, an increase in the power consumption, and an increase in the size of apparatus.

[0019] It is an object of the present invention to provide an image forming apparatus comprising (i) image data producing means for producing image data of an image on a page at constant speed, (ii) an image memory for storing image data of an image on at least one page, (ii) a code memory for storing code data of the image on said at least one page, (iv) image data writing means for writing the image data produced by the image data producing means in the image memory, and (v) coding means for reading the image data written by the image data writing means from the image memory, coding the read image data to decrease a data amount thereof, thereby obtaining code data, and then writing the code data in the code memory, said image forming apparatus being capable of shortening the time required to process a series of image pages, including writing image data into the image memory and coding and/or decoding the image data without increasing the capacity of the memory.

[0020] It is a further object to provide an image forming apparatus comprising (i) a code memory for storing code data of an image on a page or of images on pages in compressed form, (ii) an image memory for storing image data of the images on the page or of the images on the pages, (iii) decoding means for reading the image data from the code memory, decoding the read image data, and then writing the decoded image data in the image memory, (iv) image data reading means for reading the image data decoding by the decoding means from the image memory at a constant speed, (v) printing/outputting means for printing and outputting the image data of the image on the page, which is read by the image data reading means from the image memory, said image forming apparatus being capable of shortening the time required to process a series of image pages, including writing image data into the image memory and coding and/or decoding the image data without increasing the capacity of the memory.

[0021] An apparatus with features achieving the above object is defined in claim 1 or claim 7, respectively. Further embodiments are defined in the dependent claims.

[0022] According to one aspect of the present invention, there is provided an image forming apparatus comprising: reading means for reading image data from a manuscript; an image memory for storing the image data read by the reading means; writing means for writing the image data read by the reading means into the image memory; coding means for reading and coding the image data stored in the image memory and storing the coded data in a code memory; decoding means for decoding the coded data stored in the code memory and writing the decoded data into the image memory; image forming means for forming an image corresponding to the decoded image data stored by the decoding means in the image memory; and control means for not only enabling the writing operation of the writing means and the coding operation of the coding means to progress simultaneously, but also performing control so that the coding operation may not pass the writing operation.

[0023] As described above, the writing of image data from the reading means into the image memory and the coding operation of reading the image data and coding the read-out data are advanced simultaneously. This shortens the processing time needed for a series of operations including the writing of image data into the image memory and the coding of the image data, without increasing the capacity of the image memory.

[0024] According to another aspect of the present invention, there is provided an image forming apparatus comprising: reading means for reading image data from

a manuscript; an image memory for storing the image data read by the reading means; writing means for writing the image data read by the reading means into the image memory; coding means for reading and coding the image data stored in the image memory and storing the coded data in a code memory; decoding means for decoding the coded data stored in the code memory and writing the decoded data into the image memory; image forming means for forming an image corresponding to the decoded image data stored by the decoding means in the image memory; and control means for not only enabling the decoding operation of the decoding means and the image forming operation of the image forming means to progress simultaneously, but also performing the decoding means so that the image forming operation may not pass the decoding operation.

[0025] As described above, the decoding from the code memory to the image memory and the operation of reading the image data and forming an image are advanced simultaneously. This shortens the processing time needed for a series of operations including the decoding of the coded data and the operation of reading the decoded image data and forming an image, without increasing the capacity of the image memory.

[0026] This invention can be more fully understood from the following detailed description when taken in conjunction with the accompanying drawings, in which:

FIG. 1 is a general block diagram of an embodiment of the present invention;
FIG. 2 is a block diagram of the basis unit of the embodiment;
FIG. 3 is a block diagram of a system basic unit of the embodiment;
FIG. 4 is a block diagram of a system expansion unit of the embodiment;
FIG. 5 is a block diagram of the image processing circuit of FIG. 2;
FIG. 6 is a block diagram of the system control circuit of FIG. 3;
FIG. 7 is a block diagram of the communication memory access control circuit of FIG. 6;
FIG. 8 is a block diagram of the page memory access control circuit of FIG. 6;
FIG. 9 is a block diagram of the address control circuit of FIG. 3;
FIG. 10 is a block diagram of the address generator section of FIG. 9;
FIGS. 11A and 11B show examples of the direction in which addresses are generated at the address generator section of FIG. 9;
FIG. 12 shows the configuration of the FIFO address generator of FIG. 10 in detail;
FIG. 13 shows the concept of two-dimensional access to the page memory of FIG. 3;
FIG. 14 shows two-dimensional access to the page memory of FIG. 3 using linear addresses;
FIG. 15 is a block diagram of the data control circuit of FIG. 3;
FIG. 16 is a block diagram of the image data transfer control section of FIG. 15;
FIG. 17 is a block diagram of the timer;
FIG. 18 shows the configuration of the image bus priority control section of FIG. 16 in detail;
FIG. 19 shows the configuration of the page memory priority control section of FIG. 16 in detail;
FIG. 20 shows the configuration of the terminal counter of FIG. 16 in detail;
FIG. 21 schematically shows electronic sorting;
FIG. 22 shows an example of electronic sorting;
FIGS. 23A and 23B show a conventional scanner input, coding process, printer output, and decoding process;
FIGS. 24A and 24B are diagrams to help explain the operation of accessing the page memory;
FIGS. 25A and 25B shows a scanner input, coding process, printer output, and decoding process by software control;
FIG. 26 is a flowchart for coding control;
FIG. 27 is a flowchart for coding control;
FIG. 28 is a flowchart for decoding control;
FIG. 29 is a flowchart for decoding control;
FIGS. 30A and 30B show a scanner input, coding process, printer output, and decoding process by hardware;
FIG. 31 is a flowchart for coding control;
FIG. 32 is a flowchart for decoding control;
FIGS. 33A to 33D show FIFO control in coding; and
FIGS. 34A to 34F show FIFO control in decoding.

[0027] Hereinafter, an embodiment of the present invention will be explained by reference to the accompanying drawings.

[0028] FIG. 1 is a block diagram of the entire configuration of an image forming apparatus. The image forming apparatus comprises the following three systems: a basic unit 1 that executes a basic copying function; a system basic unit 2 that has a page memory that temporarily stores image data when the apparatus is connected to another system or when the image data is edited, processed, and copied; and a system expansion unit 3 that has not only an optical disk for optically semipermanently storing the image data entered from the basic unit 1, but also control means for converting image data and control data into those suited for the control system and image format of another system when the image data and control data are exchanged with another system.

[0029] The basic unit 1 and the system basic unit 2 are connected to each other by means of a basic section system interface 4 that enables exchange of control data between these two units and a basic section image interface 5 that enables exchange of image data between these two units.

[0030] The system basic unit 2 and the system expansion unit 3 are connected to each other by means of an

expansion section system interface 6 that enables exchange of control data between these two units and an expansion section image interface 7 that enables exchange of image data between these two units.

[0031] That is, the basic unit 1 is not connected directly to the system expansion unit 3. Whenever control data and image data are exchanged between these two units, they pass through the system basic unit 2.

[0032] The image forming apparatus takes three forms, depending on whether it is connected to the system basic unit 2 and/or the system expansion unit 3.

[0033] Specifically, a first form is a configuration consisting of the basic unit 1 only. With this configuration, the basic function is a copying function and enables a copying process involving simple editing processes, including an enlarging/reducing process and a masking/trimming process.

[0034] A second form is such that the system basic unit 2 is connected to the basic unit 1. In addition to the copying function of the basic unit 1, the second form enables editing processes including an image rotating process and the process of combining images. The system basic unit 2 is designed to connect to a FAX (facsimile) unit 8 constituting communication channel control means, such as a facsimile, and a printer controller 9 that enables the printer for the basic unit 1 to be used as a remote printer for a control apparatus, such as an external personal computer, as well as to the system expansion unit 3. It is possible to transmit images from the FAX unit 8 to another system or apparatus via a communication channel or conversely to cause the FAX unit to receive the image data from another system or apparatus via a communication channel. The received image data is sent to the basic unit 1 and printed out on a printer explained later.

[0035] A third form is the form shown in FIG. 1, where the basic unit 1, system basic unit 2, and system expansion unit 3 are connected to each other.

[0036] In addition the functions of the first and second forms, the third form has a data storage/management function that optically semipermanently stores the image data and manages the stored image data, a LAN image data transmitting/receiving function that causes local area network (LAN) channel control means, which will be explained later, to transmit images to another system or apparatus via a LAN channel or conversely to receive the image data from another system or apparatus via a LAN channel, and a printer function that converts the print control code transmitted from a personal computer via a general-purpose interface into image data and prints out the image data on the printer of the basic unit 1 via the page memory of the system basic unit 2.

[0037] The basic unit 1, as shown in FIG. 2, comprises a system CPU 11 constituting the body of the control section, a control panel 12 provided with an operator section and a display section, an image scanner 13 serving as input means for reading images from a manuscript, an image processing circuit 14, and a printer 15 serving as output means. The system CPU 11 is connected via a basic section system bus 16 to a control panel 12, a scanner 13, an image processing circuit 14, and a printer 15 serving as output means for providing image forming output, and controls these. The basic section system bus 16 is connected to the basic section system interface 4.

[0038] The scanner 13 has a CCD line sensor (not shown) composed of light-receiving elements arranged in a line and reads the image of a manuscript put on a manuscript table (not shown) line by line according to the instruction from the system CPU 11, converts the shades of the image into 8-bit digital data, and then outputs the digital data together with a synchronizing signal as time-sequential digital data to the image processing circuit 14 via a scanner interface.

[0039] The printer 15 is made up of an image forming section (not shown) which is a combination of a laser optical system (not shown) and an electrophotograhic system capable of forming images on transfer paper. According to the instruction from the system CPU 11, the printer takes in the 4-bit digital image data from the image processing circuit 14 via a printer interface in synchronization with the synchronizing signal, forms an electrostatic latent image on a photosensitive drum (not shown) by a laser beam whose pulse width is proportional to the size of the image data, makes the electrostatic latent image visible by visualizing means (not shown), transfers the visualized image onto transfer paper by transfer means (not shown), fixes the image on the transfer paper by fixing means, and then outputs the transfer paper.

[0040] The control panel 12 is composed of an operator section for setting the operation mode of the apparatus and parameters and a display section that displays the state of the system or the image data stored in the page memory in the system basic unit 2. The system CPU 11 also controls each section of the system basic unit 2 explained later.

[0041] The image processing circuit 14, as shown in FIG. 5, comprises a smoothing edge-emphasizing circuit 141, an editing/moving circuit 142, an enlarging/reducing circuit 143, and a gray level transformation circuit 144.

[0042] The smoothing edge-emphasizing circuit 141 removes noise introduced in reading images at a smoothing circuit and sharpens the edges dulled due to smoothing at an edge emphasizing circuit.

[0043] The editing/moving circuit 142 performs simple editing processes line by line, including a moving process along a line and a masking/trimming process.

[0044] The enlarging/reducing circuit 143 performing the process of repeating pixels according to the specified magnification or an enlarging/reducing process by a combination of a curtailing process and an interpolating process.

[0045] The gray level transformation circuit 144 trans-

forms the image data with 8 bits per pixel read by the scanner 13 into a specified number of gray levels by area gray level techniques. The gray-level-transformed image data is image data with 4 bits per pixel, the number of bits used on a printer. The image data is sent to the printer 15 or to the system basic unit 2 via the scanner data bus 17 and the basic section image interface 5. The nonlinearity of the input/output characteristic of the printer 15 is corrected by the area gray-level techniques at the same time that the gray-level process is performed.

[0046] The system basic unit 2, as shown in FIG. 3, comprises a page memory 28 that stores image data temporarily, a system control circuit 21 that controls the accessing of the basic unit 1 and system expansion unit 3 to the page memory 28, a page memory address control circuit 26 that generates addresses for the page memory 28, an image bus 29 that performs data transfer between the individual devices in the system basic unit 2, and a page memory data control circuit 27 that controls data transfer in performing data transfer between the page memory 28 and another device via the image bus 29.

[0047] The system basic unit 2 further comprises an image data I/F 210 that interfaces image data when the system basic unit exchanges image data with the basic unit 1 via the basic section image interface 5, a resolution conversion binary rotation circuit 212 that converts the image data into that with a resolution suitable for another apparatus when the image data is transmitted to the apparatus with a different resolution, converts the image data received from an apparatus with a different resolution into that with a resolution suitable for the printer 15 of the basic unit 1, or rotates the binary image data 90 degrees, and a compression/expansion circuit 211 that compresses the input image data for facsimile transmission and optical disk storage where the image data is compressed and transmitted or stored, and that expands the compressed image data for the printer 15 to visualize the data.

[0048] The system basic unit 2 further comprises a FONT memory in which character fonts are stored, a work memory that temporarily stores control information used in the system CPU 11, a system memory (ROM/RAM) 24 composed of a program memory in which processing programs used to perform processes using the system basic unit 2 are stored, a system DMA controller 23 that enables high-speed data transfer between devices in the basic section system bus 16, and a printer controller interface 213 that interfaces not only control information when the printer controller 9 exchanges the control signal with the system CPU 11, but also image data when the printer controller 9 exchanges the image data with the image bus 29.

[0049] The system basic unit 2 further comprises a system control circuit 21, a communication memory 25 in which control information is stored when control information is exchanged between the system CPU 11 and the CPU of the system expansion unit 3, an image data I/F 210, and a multivalue rotation memory 214 used to rotate the image data 90 degrees or 180 degrees and output the resulting data to the printer 15. The FAX unit 8 and printer controller 9 are connected optionally.

[0050] The system expansion unit 3, as shown in FIG. 4, comprises an expansion CPU 31 that controls each of the other devices within the unit 3 via an expansion system device 43, an expansion DMA controller 32 that controls data transfer on the expansion section system bus 43, a general-purpose ISA bus 44, an ISA bus controller 33 that interfaces the expansion section system bus 43 with the ISA bus 44, storage means that is connected to the expansion section system bus 43 and electronically stores image data, such as a hard disk unit 35, a hard disk interface 34 for the storage means, storage means that is connected to the ISA bus 44 and optically stores image data, such as an optical disk unit 38, an optical disk interface 37 for the preceding storage means, a local area network channel control unit (LAN) 41 for achieving a LAN function, a printer controller control unit 40 for achieving a printer function, a G4 FAX control circuit 39 having a G4 FAX control function, an expansion SCSI interface 42 used to connect to a SCSI device, an expansion section image bus 45 that enables the printer controller control unit 40 to output image data to the system basic unit 2 via the expansion image interface 7, and a buffer memory 36 that interfaces when the expansion section system bus 43 exchanges data with the expansion section image bus 45.

[0051] The optical disk interface 37, optical disk unit 38, G4 FAX control circuit 39, printer controller control unit 40, local area network channel control unit 41, and expansion SCSI interface 42 are optional devices and can be installed in and removed from the system expansion unit 3.

[0052] The optical disk unit 38 is connected to the ISA bus 44 via the interface 37. The expansion CPU 31 controls the optical disk unit 38 via the expansion section system bus 43, ISA bus controller 33, and ISA bus 44, using a SCSI command.

[0053] The local area network channel control unit 41 comprises a channel control section that controls the communication of control data and image data with other devices on the network on the basis of the protocol of the connected network system, a common memory in which the communication control data and image data from the LAN or the control data and image data from the system expansion bus are temporarily stored, and a system expansion bus interface.

[0054] The printer controller control unit 40 comprises a parallel interface that exchanges control code and image data with a personal computer and conforms to a centronics interface, a system expansion image bus interface that interfaces with the system expansion section image bus 45 for transferring the bit image data to the page memory 28 of the system basic unit, an image data transfer control section that controls transfer of im-

age data in the apparatus, control means that interprets the control code from a personal computer and tells the control information to the expansion CPU 31 via the expansion section system bus 43 and ISA bus 44 or that interprets the print control code from a personal computer, converts it into bit information, and then stores the bit information in the memory of the apparatus, and a system expansion bus interface that interfaces with the ISA bus 44.

[0055] The configuration and function of the important portion of the system basic unit 2 will be explained in detail.

[0056] The system control circuit 21, as shown in FIG. 6, comprises a communication memory access control circuit 401 that controls the communication of control information between the system CPU 11 and the expansion CPU 31, a communication memory interface 402 that interfaces with the communication memory 25, a page memory access control circuit 403 that controls the accessing of the basic unit 1 and system expansion unit 3 to the page memory 28, a basic section system bus interface 405 that decodes the address received together with the control information and image information sent from the system CPU 11 of the basic unit 1 via the basic section system bus 16 and allocates the control information and image information to the relevant block in the system basic unit 2, a system expansion bus interface 406 that decodes the address received together with the control information and image information sent from the system expansion unit 3 and allocates the control information and image information to the relevant block in the circuit, and a page memory interface 404 that interfaces exchange of image data between the page memory access control circuit 403 and the page memory 28, when the means (the CPU 11 and DMA controller 23 in the basic unit) capable of page memory accessing on the basic section system bus 16 and the means (the CPU 31 of the system expansion unit 3 and the DMA controller 32) capable of page memory accessing on the system expansion bus 43 each access the image information in the page memory 28 via the system bus.

[0057] The communication memory access control circuit 401 controls the accessing of the communication memory 25 when the CPU 11 of the basic unit 1 and the CPU 31 of the system expansion unit 3 exchange control code with the communication memory 25 via the communication memory interface 402 in the system control circuit 21.

[0058] The communication memory 25 has been mapped in the memory space of the CPU 11 of the basic unit 1 and that of the CPU 31 of the system expansion unit. When each CPU accesses a particular area, it can read the data from and write the data into the communication memory 25.

[0059] The communication memory access control circuit 401, as shown in FIG. 7, comprises a mediation circuit 410, a communication memory access sequencer 412, a bi-directional selector 413, and an interrupt control circuit 414.

[0060] The mediation circuit 410 provides communication memory access priority control of the CPU 11 of the basic unit 1 and the CPU 31 of the system expansion unit 3. When the CPU 11 of the basic unit 1 and the CPU 31 of the system expansion unit 3 have accessed the communication memory 25 at the same time, the mediation circuit 410 allows one to access the memory and forces the other to wait for access. When the mediation circuit 410 has received an access request from the other CPU while one CPU is accessing the communication memory 25, it forces the other CPU to wait for access. The communication memory access sequencer 412 outputs a read or write control signal to the communication memory 25 on the basis of the request of the allowed CPU.

[0061] On the basis of the mediation result, the bi-directional selector 413 supplies to the communication memory 25 the address in the communication memory 25 outputted from the allowed control means, in synchronization with the timing signal outputted from the communication memory access sequencer 412. In a write operation, the selector supplies to the communication memory 25 the communication information (data) outputted together with the address from the allowed CPU as well as the address information. In a read operation, the selector receives the address in the communication memory 25 from the allowed CPU and the communication information read from the communication memory 25 in synchronization with the timing signal outputted from the communication memory access sequencer 412, and supplies them to the allowed CPU.

[0062] The page memory access control circuit 403, as shown in FIG. 8, comprises a mediation circuit 430, data registers 431, 432, 436, 437, an address register 433, a bi-directional selector 434, and a page memory access sequencer 435.

[0063] The mediation circuit 430 provides page memory access priority control of the CPU 11 of the basic unit 1 and the CPU 31 of the system expansion unit 3. When the CPU 11 and the CPU 31 have accessed the page memory 28 simultaneously, the mediation circuit 430 allows one CPU to access the page memory according to the priority given to them and forces the other CPU to wait for access.

[0064] On the basis of the request of the allowed CPU, the page memory access sequencer 435 outputs to the address control circuit 26 a control signal for reading or writing the data from or into the page memory 28.

[0065] On the basis of the mediation result of the mediation circuit 430, the bi-directional selector 434 supplies to the address control circuit 26 the address in the page memory 28 outputted from the allowed CPU, in synchronization with the timing signal outputted from the page memory access sequencer 435. In a write operation, the selector supplies to the data control circuit 27 the information (data) outputted together with the ad-

dress from the allowed CPU as well as the address information. In a read operation, the selector receives via the data control circuit 27 the address in the page memory 28 from the allowed CPU and the information (data) read from the page memory 28 in synchronization with the timing signal outputted from the page memory access sequencer 435, and supplies them to the allowed CPU.

[0066] The data register 431 and data register 432 are registers that temporarily store the data when the basic unit 1 accesses the page memory 28. The address register 433 is a register that temporarily stores the address in the page memory 28 outputted from the basic unit 1.

[0067] When the basic unit 1 accesses the page memory 28 using the data register 431, the address outputted from the basic unit 1 is temporarily stored in the address register 433 and then outputted to the page memory 28 via the address control circuit 26. In contrast, the basic unit 1 accesses the page memory using the data register 432, the address outputted from the basic unit 1 is ignored and the address generator section of the address control circuit 26 outputs an address to the page memory 28 on the basis of the setting information.

[0068] The data register 436 and data register 437 are registers that temporarily store the data when the system expansion unit 3 accesses the page memory 28. When the system expansion unit 3 accesses the page memory 28, the address generator section of the address control circuit 26 outputs addresses to the page memory 28 on the basis of the setting information.

[0069] The system DMA controller 23 of the system basic unit 2 is a controller for transferring the data between devices on the basic section system bus 22 at high speeds from the viewpoint of hardware, without intervention of the CPU 11 of the basic unit 1.

[0070] The processes of transferring data by the use of the system DMA controller 23 include the transferring of compressed data (coded data) between the page memory 28 and the FAX unit 8 in the FAX transmitting/receiving process, the transferring of image data between the page memory 28 and the control panel 12 to display the image in the page memory 28 at the control panel 12, and the transferring of data between the system memory 24 and the control panel 12 to display an operation screen at the control panel 12.

[0071] The address control circuit 26 that generates addresses in the page memory 28, as shown in FIG. 9, comprises a transfer control sequencer 610 that executes various types of transfer sequence according to the request from the image bus, a mediation section 611 that mediates between a request for use of image bus and a request for use of system bus, an address generator section 612 that generates various memory addresses in a plurality of channels in transferring from the image bus, a selector 613 that switches between the addresses outputted from the address generator section 612 and the system addresses, and a DRAM control section 614 that generates addresses in the DRAM and its control signals.

[0072] The address control circuit 26 accepts memory access requests from the two routes of the image bus and the system bus. These requests are arbitrated at the mediation section 611 and the data transfer process on the bus given priority over the other is performed.

[0073] When the system bus' request has been given priority, the system address selected by the selector 613 is inputted to the DRAM control section 614. The DRAM control section 614 not only converts the entered address into an address in the DRAM, but also generates the control signal necessary for reading and writing.

[0074] The transfer control sequencer 610, to which the request, together with the address channel signal, is inputted from the image bus, selects one of the address generators in the address generator section 612. When the image bus' request has been given priority, the memory address in the selected channel is outputted from the address generator section 612 and inputted to the DRAM control section 614.

[0075] The address generator section 612, as shown in FIG. 10, comprises four channels of two-dimensional address generators 631, 632, 633, 634, and two channels of FIFO address generators 635, 636, and a selector 637 that selects one of the generated memory addresses according to the channel select signal from the transfer sequencer.

[0076] The two-dimensional address generators 631 to 634 can generate various types of addresses. For example, as shown in FIG. 11A, they can generate addresses one after another in the X direction in synchronization with the clock from the transfer control sequencer. Furthermore, by changing parameters, they can generate addresses sequentially in the direction opposite to the Y direction as shown in FIG. 11B. In addition, the start address or the main scanning width (XW) of a single line can be set arbitrarily according to the size of a sheet of manuscript paper.

[0077] Use of the two-dimensional address generators that can generate various types of addresses enables the transfer of data to a given rectangular area in the page memory 28, rotational reading, and repetitive reading. Furthermore, use of two channels of two-dimensional address generators enables image editing, including the movement of an image between any areas in the page memory 28, the rotation of an image, length-to-breadth conversion, repetition, and mirror image.

[0078] The FIFO address generators 635, 636 generate FIFO addresses for using the page memory 28 as a FIFO memory and the statuses necessary for FIFO control. The statuses include FIFO full (the status where the FIFO area is full of unread data) and FIFO empty (the status where the FIFO area has no unread data). By reading the contents from the FOFO register, the amount of data in the FIFO and the empty capacity can be known.

[0079] By performing FIFO control using these statuses, it is possible to absorb the difference in transfer

speed or transfer timing when the data is transferred from one device to another on the image bus 29 or from a device on the image bus 29 to the system bus 22, enabling high-speed data transfer. The FIFO address generators 635, 636 can be used as a one-dimensional address generator for two channels for a single channel (a single circuit) when FIFO control is not performed.

[0080] A detailed configuration of the FIFO address generators 635, 636 will described by reference to FIG. 12. Each FIFO address generator is composed of one-dimensional address generator channels A4601 and B4603, start address setting units A4602 and B4604 that give start addresses to the one-dimensional address generators, respectively, an FIFO status generator 4605, and an FIFO area size setting unit 4606.

[0081] The one-dimensional address generator 4601 is counted up by a count-up signal each time a transfer has ended. This makes it possible to write or read the data into or from consecutive addresses in the memory.

[0082] The address generators 635, 636 have two modes: one mode in which consecutive one-dimensional addresses are generated, and the other mode in which addresses are generated so as to make a loop in such a manner that when addresses are generated, starting at the start address, and reach the size of the FIFO area, then the address is returned to the start address in the next transfer.

[0083] In the FIFO address mode, one channel has a write address generated for FIFO control and the other channel has a read address generated for FIFO control.

[0084] The FIFO status generator generates a status indicating the statuses of the data in the FIFO area on the basis of the addresses of the two channels and the size of the FIFO area. The statuses include two statuses: FIFO full and FIFO empty.

[0085] FIFO full indicates the status in which the FIFO area is full of unread data. Since data cannot be written in any more, the writing of data is inhibited using the FIFO full signal.

[0086] FIFO empty indicates that the FIFO area has no unread data and data cannot be read any more, so that the reading of data is inhibited by using the FIFO empty signal.

[0087] Thus, by performing transfer control in the FIFO address mode, part of the memory can be used as the FIFO area to absorb the difference in speed between the reading and writing operations, thereby enabling high-speed data transfer.

[0088] FIG. 13 is a conceptual diagram for two-dimensional access to the page memory 28.

[0089] If the width of an access to the page memory 28 (in the figure, 64 bits) is a column, a line will consist of an integral multiple of a column. Consecutive columns in the X direction in the same line have consecutive linear addresses in the page memory 28, with the linear address of the last column in the line and that of the first column in the next line being consecutive.

[0090] FIG. 14 illustrates the two-dimensional memory of the page memory 28 of FIG. 13 using linear addresses.

[0091] The data control circuit 27, as shown in FIG. 15, comprises an image data transfer control section 701 that controls data transfer between devices on the image bus 29 in the system basic unit 2 and data transfer between devices on the image data bus 29 and the page memory 28, an image processing section 702 that executes bit block transfer and various raster operations (logical operations), a system interface 703 that interfaces data when the CPU 11 of the basic unit 1 or the CPU 31 of the system expansion unit 3 accesses (reads and writes from and into) the page memory 28 via the system control circuit 21, a selector 704 that selects either the data on the image bus 29 transmitted via the image data transfer control section 701 or the data from the CPU (the CPU 11 of the basic unit 1 or the CPU 31 of the system expansion unit 3) via the system interface 703, on the basis of the page memory access mediation result of the address control circuit 26 in writing the data into the page memory 28, and a selector 705 that selects either the sending of the data to the image bus 29 via the image data transfer control section 701 or the sending of the data to the CPU (the CPU 11 of the basic unit 1 or the CPU 31 of the system expansion unit 3) via the system interface 703, on the basis of the page memory access mediation result of the address control circuit 26 in reading the data from the page memory 28.

[0092] Explained next will be the control operation of the image data transfer control section 701 shown in FIG. 15. The image data transfer modes that the image data transfer control section 701 controls are the following two.

[0093] One mode is data transfer between I/O devices on the image bus 29 in the system basic unit 2, with both the source (the device transferring the data) and the destination (the device receiving the data) on the image bus 29, and is composed of two cycles: a read cycle in which the data is loaded from the source into the data buffer in the image data transfer control section 701 and a write cycle in which the data on the data buffer is written into the destination.

[0094] The other mode is data transfer between I/O devices on the image bus 29 in the system basic unit 2 and the page memory 28 and is made up of two cycles: a data transfer cycle in which the data is transferred between an I/O device and the data buffer in the image data transfer control section 701 and a data transfer cycle in which the data is transferred between the data buffer and the page memory 28.

[0095] Since the section between the page memory 28 and the data buffer is independent of the image bus 29, the two cycles can operate in parallel. The image data transfer control section 701 can specify two modes of data transfer for eight channels and transfer data in eight channels at the same time.

[0096] The image data transfer control section 701, as shown in FIG. 16, comprises a data buffer 740, an

image bus priority control section 741, a transfer control sequencer 742, a page memory priority control section 743, a page memory timing control section 744, a terminal counter 745, an interrupt control section 746, a control bus interface 747, a parameter register 748, and an I/O buffer 749.

[0097] The data buffer 740 has as many data registers for temporarily storing the data from the source in data transfer as there are channels. The image bus priority control section 741 receives a data transfer request (REQ) from a device on the image bus 29, determines a device allowed to transfer data by specific priority control, tells the allowed device that it is allowed to start data transfer.

[0098] The transfer control sequencer 742 generates a timing signal of data transfer between the source device determined on the basis of the priority control result of the image bus priority control section 741 and the destination device, and outputs the timing signal to the image bus 29. The page memory priority control section 743 receives the request signal outputted from the data buffer 740 and determines a data transfer channel between the page memory 28 and the data buffer 740 on the basis of specific priority.

[0099] The page memory timing control section 744 generates a timing signal of data transfer between the page memory 28 in the transfer channel determined on the basis of the priority control result of the page memory priority control section 743 and the data buffer 740, and outputs the timing signal to the address control circuit 26. In the process of writing the data into the page memory 28, the transfer request signal from the data buffer 740 is outputted to the page memory priority control section 743 in the state where the data from a device on the image bus 29 is stored in the data buffer 740, whereas in the process of reading the data from the page memory 28, the transfer request signal is outputted to the page memory priority control section 743 when no data is stored in the data buffer 740. The parameter register 748 is a register in which the following items are set for each transfer channel: the device transferring the data, the device receiving the data, the number of bytes transferred, and the presence or absence of an interrupt process after the completion of transfer.

[0100] The image bus 29 has a data width of 32 bits and always performs 32-bit data transfer, regardless of a bit width of a single pixel. For instance, when binary (a bit/pixel) data is written from the scanner 13 into the page memory 28, the 32-pixel data is transferred from the image data I/F 210 to the page memory 28 at a time on the image bus 29 via the image data transfer control section 701. In addition, when multivalued data (four bits/pixel) is written into the page memory 28, data of eight pixels is transferred at a time on the image bus 29. Converting data into 32-bit data is effected according to the number of bits per pixel at each device on the image bus 29.

[0101] Data transfer priority control on the image bus 29 is such that priority is determined on the basis of the nature of a device in such a manner that a transfer request from a device which can neither stop data transfer in the middle nor wait for data transfer as found in the process of outputting data to the printer or the process of inputting data from the scanner, is allowed preferentially, and that a transfer request from a device which can wait for data transfer as found in the compression/expansion process or the resolution conversion process, is allowed only when there is no transfer request from a device with a higher priority level.

[0102] A timer 900 is connected to the system bus 16 of FIG. 2. The timer 900 is composed of a timer control section 901, a reference clock generator circuit 202, a reference clock frequency demultiplier 903, and a down counter 904.

[0103] The timer control section 901 sets a frequency division ratio in the reference clock frequency demultiplier 903 and controls the start and stop of counting at the down counter 904. Additionally, the timer control section 901 can generate an interrupt signal to the system CPU 11 in response to the carry down signal outputted from the down counter 904.

[0104] The reference clock generator circuit 902 generates an accurate 25-MHz square wave using a crystal oscillator. On the basis of the setting from the system CPU 11, the reference clock frequency demultiplier 903 divides the reference clock into a frequency of 1/n at frequency ratios ranging from 1/1 to 1/65536.

[0105] The down counter 904 is a 32-bit binary down counter, which counts down in synchronization with the frequency division clock. The initial value of the down counter 904 is set by the system CPU 11 via the system bus 16.

[0106] When a carry-down (carrying down from 0) takes place in the down counter 904, the preceding initial value set by the system CPU 11 is set automatically. The value in the down counter 904 can be read from the system CPU 11 any time via the system bus 16. The start and stop of counting down at the down counter 904 are controlled by the count enable signal outputted from the timer control section 901.

[0107] A detailed configuration of the image bus priority control section 741 of FIG. 16 will be explained by reference to FIG. 18. The image bus priority control section 741 comprises an image bus transfer request mediation section 910, request mask circuits 911 for eight channels, and request generator sections 912 for eight channels.

[0108] An image bus transfer request signal and a channel buffer status are inputted to each of the request generator sections 912, which are independent of each other, one transfer channel to another. When the conditions for the two are fulfilled, an internal valid transfer request is generated. The image bus transfer request signal is a signal made active when a device connected to the image bus 29 requests data transfer on the image bus 29. The channel buffer status is a signal indicating

the state of the data buffer 740 for data exchange in each transfer channel and has two states: an "empty" state in which no effective data is in the data buffer in the channel and a "full" state in which effective data is in the data buffer.

[0109] In the case of device read transfer from a device on the image bus 29 to the data buffer 740, when the status of the data buffer in the channel to which the data is to be transferred is "empty" and the request signal from the device to the channel is active, an internal valid transfer request is generated by the request generator section 911.

[0110] In the case of device write transfer from the data buffer 740 to the image bus, when the data buffer in the channel to which the data is to be transferred has valid data, the buffer status is "full", and the request signal from the device to the channel is active, a valid transfer request is generated by the request generator section 912.

[0111] The request mask circuit 911 determines whether or not the transfer request generated at the request generator section in the preceding stage is made valid. The transfer channel enable determines whether or not transfer through the channel is permitted.

[0112] The TC mask is for transfer amount control and sets the number of words to be transferred in the terminal counter 745 in advance. After a specified number of words has been transferred, the TC mask becomes active, inhibiting transfer through the channel. When the transfer amount control is not performed, the setting is done so that the TC mask may always be inactive.

[0113] The FIFO control mask determines whether or not transfer through the channel is permitted in performing FIFO control. When the FIFO control mask is active, this inhibits transfer; and when the mask is inactive, this permits transfer.

[0114] On the basis of the setting from the system CPU 11, it is determined whether FIFO control is effected according to the FIFO status from the FIFO address generators 635, 636 or to the comparison result of the transfer comparator in the terminal counter 745, or FIFO control is not performed.

[0115] When FIFO control is not effected, the FIFO control mask is always made inactive by the setting.

[0116] The image bus transfer request mediation section 910 arbitrates transfer requests in eight channels generated at the request mask circuit 911, chooses one channel, and outputs to a device in the selected channel an image bus transfer acknowledge signal that indicates that the request has been accepted and transfer has been permitted. The device that has received the acknowledge signal performs data transfer on the image bus 29.

[0117] Mediation priority control effected when transfer requests have occurred in a plurality of channels is based on round robin scheduling control in which the priority level of the channel through which the last transfer has been performed is the lowest, with the channel 1 to channel 8 arranged in a ring. Thus, even if all of the eight channels are making requests, each channel is allowed equally to perform transfer because a turn to transfer never fails to come to each channel until eight transfers have been completed.

[0118] Now, a detailed configuration of the page memory priority control section 743 of FIG. 16 will be described by reference to FIG. 19. The page memory priority control section 743 is composed of the page memory transfer request mediation section 921, request mask circuits 922 for eight channels, and request generator sections 923 for eight channels.

[0119] A channel buffer status is inputted to each of the request generator sections 923, which are independent of each other, one transfer channel to another. When the condition for the channel buffer status is fulfilled, an internal valid transfer request is generated.

[0120] The channel buffer status is a signal indicating the state of the data buffer 740 for data exchange between the individual transfer channels and has two states: an "empty" state in which the data buffer in the channel has no valid data and a "full" state in which the data buffer has valid data.

[0121] In the case of memory read transfer from the page memory 404 to the data buffer 740, when the status of the data buffer in the channel to which the data is to be transferred is "empty", that is, data exchange is possible, an internal valid transfer request is generated by the request generator section.

[0122] In the case of memory write transfer from the data buffer 740 to the page memory 404, when the data buffer in the channel to which the data is to be transferred has valid data and the buffer status is "full", an internal valid transfer request is generated by the request generator section 923.

[0123] The request mask circuit 922 determines whether or not the transfer request generated at the request generator section in the preceding stage is made valid. The transfer channel enable determines whether or not transfer through the channel is permitted.

[0124] The TC mask is for transfer amount control and sets the number of words to be transferred in the terminal counter 745 in advance. After a specified number of words has been transferred, the TC mask becomes active, inhibiting transfer through the channel. When the transfer amount control is not performed, the setting is done so that the TC mask may always be inactive.

[0125] The FIFO control mask determines whether or not transfer through the channel is permitted in performing FIFO control. When the FIFO control mask is active, this inhibits transfer; and when the mask is inactive, this permits transfer.

[0126] On the basis of the setting from the system CPU 11, it is determined whether FIFO control is effected according to the FIFO status from the FIFO address generators 635, 636 or to the comparison result of the transfer comparator in the terminal counter 745, or FIFO control is not performed. When FIFO control is not ef-

fected, the FIFO control mask is always made inactive by the setting.

[0127] The page memory transfer request mediation section 921 arbitrates transfer requests in eight channels generated at the request mask circuit 922, chooses one channel, and outputs to the address control section 26 a select signal (RCHN) for the address generator set in the selected channel.

[0128] Mediation priority control effected when transfer requests have occurred in a plurality of channels is based on round robin scheduling control in which the priority level of the channel through which the last transfer has been performed is the lowest, with the channel 1 to channel 8 arranged in a ring. Thus, even if all of the eight channels are making requests, each channel is allowed equally to perform transfer because a turn to transfer never fails to come to each channel until eight transfers have been completed.

[0129] Now, a detailed configuration of the terminal counter 745 of FIG. 16 will be explained by reference to FIG. 20. The terminal counter 745 counts the number of words transferred for each channel and is made up of a count down generator section 931, number-of-transferred-words counters 932 for eight channels, four number-of-transfers comparators each connected to two channels.

[0130] The count down signal generator 931 outputs a count down signal to the number-of-transferred-words counter 932 for the selected channel according to the transfer channel signal on the basis of the mediation result at the image bus priority control section 741 and the transfer end signal.

[0131] The number-of-transferred-words counter 932 is a 32-bit binary down counter which is counted down each time a single transfer in the channel on the image bus 29 has ended. The initial value in the counter 745 is set by the system CPU 11 via the system bus 16. When a carry-down (carrying down from 0) has taken place, a terminal count signal is outputted. The value of the number-of-transferred-words counter 932 can be read from the system CPU 11 any time via the system bus 16.

[0132] The interrupt mask circuit 934 permits the terminal count signals for eight channels to interrupt the system CPU or inhibits the terminal count signals from interrupting the system. The interrupt mask circuit ORs the terminal count signals into a single signal and outputs the resulting signal as a terminal count interrupt signal. The setting of permitting or inhibiting each channel is effected by the system CPU 11.

[0133] The number-of-transfers comparator 933 compares the number of transferred words in two channels and, when these numbers are equal, makes the output active as the comparison result. The comparison result is used as a control signal in performing FIFO control between the two channels.

[0134] Hereinafter, the operation of the embodiment of the present invention constructed as described above will be explained. First, the basic operation of inputting the image data from the scanner 13 to the page memory 28 will be described. The image output data with 8 bits/pixel on a manuscript read by the scanner 13 is transferred to the image data interface 210 in the form of scanner image data with 8 bits/pixel, 4 bits/pixel, 2 bits/pixel, or 1 bit/pixel via the image processing circuit 14. The image data interface 210 collects pixels (4, 8, 16, and 32 pixels) of the scanner image data and performs DMA transfer of these data items as transfer data to the data control circuit 27 in units of 32 bits via the image bus 29. The data control circuit 27 writes the 32-bit scanner image data into an address in the page memory 28 generated at the address control circuit 26.

[0135] Now, the process of compressing image data on the page memory 28 will be explained. The page memory 28 is logically divided into an image area in which image data is stored and a code area in which compressed code data is stored.

[0136] The following two channels are set as transfer paths in the image data transfer control section 701: one channel for the image input from the image area in the page memory 28 to the compression/expansion circuit 211 and the other channel for the code output from the compression/expansion circuit 211 to the code area of the page memory 28. By determining the destination to which the code output is transferred to be the hard disk interface 34 or the optical disk interface 37, a large amount of images can be recorded on a recording medium whose unit price per bit is lower.

[0137] After the various settings of the compression process have been made in the compression/expansion circuit (coding/decoding means) 211, the coding start instruction is executed. The image data is read from the page memory 28 and inputted to the compression/ expansion circuit 211. The compression/expansion circuit 211 codes the image and outputs the codes to the code area of the page memory 28.

[0138] Now, the process of expanding the coded image data into the page memory 28 will be explained. The following two channels are set as transfer paths in the image data transfer control section 701: one channel for the code input from the code area in the page memory 28 to the compression/expansion circuit 211 and the other channel for the image output from the compression/expansion circuit 211 to the image area of the page memory 28. By determining the device from which the code input is transferred to be the hard disk interface 34 or the optical disk interface 37, a large amount of images stored in a recording medium whose unit price per bit is lower can be recorded. After the various settings for the expansion process have been made in the compression/expansion circuit 211, a decoding start instruction is executed.

[0139] The code data is read from the page memory 28 and inputted to the compression/expansion circuit 211. Then, the compression/expansion circuit 211 decodes the images and outputs the image data to the im-

age area of the page memory 28.

[0140] Now, the process of outputting the data from the page memory 28 to the printer 15 will be described. First, the image data is outputted from the page memory 28 to the printer 15. After the image data in units of 32 bits specified by the address in the page memory 28 generated at the address control circuit 26 has been transferred to the data control circuit 27, it undergoes DMA transfer to the image data interface 210 via the image bus 29.

[0141] The image data interface 210 converts the 32-bit image data into image data with 4 bits/pixel, 2 bits/pixel, or 1 bit/pixel and transfers the converted data to the printer 15 via the image processing section 14.

[0142] As described above, the basic operations, including the operation of inputting the image from the scanner 13 to the page memory 28, the image data compression process on the page memory 28, the process of expanding the coded image data onto the page memory 28, and the operation of outputting the data from the page memory 28 to the printer 15, are performed.

[0143] Now, electronic sorting will be described by reference to FIGS. 21 and 22. Electronic sorting is such that a plurality of manuscripts to be sorted are read and temporarily stored in an auxiliary storage device, such as a semiconductor memory, a hard disk, or an optical disk, and as many pages of the stored images as needed are outputted in arbitrary sequence. This makes it possible to arrange the sequence of pages of print output by outputting later inputted pages earlier or output copies of the documents in ascending order of pages. FIG. 22 illustrates an example of electronic sorting. When four manuscripts are inputted sequentially as shown in the figure, the necessary number of copies are outputted, starting with the last inputted manuscript. Because sheets of paper on which later inputted manuscripts have been printed are stacked earlier in the case of group output, the sheet of paper on which the first inputted manuscript has been printed is laid on the top of the stack. On the other hand, in the case of sorting output, a copy of the manuscripts is outputted in the reverse order of the manuscript input. The series of operations are repeated as many times as the number of copies needed.

[0144] Before explanation of the compression (coding)/ expansion (decoding) operation according to the present invention, the compression/expansion operation in the prior art will be explained by reference to FIGS. 23A and 23B. FIG. 23A shows the timing for the scanner input and coding process. As shown in FIG. 23A, to code and store the image inputted from the scanner in a page of image memory in the prior art, after a page of image was inputted from the scanner into the image memory, coding was started. At the time when the coding of the page of image was completed, the scanner started to input the next page.

[0145] Specifically, since the scanner input and the coding process were performed altemately, the coding process was stopped during the scanner input, whereas the scanner input was stopped during the coding process. This produced a dead time Td during which scanner input was not effected at all and a dead time Tc during which the coding process was not effected at all, degrading the performance of the system.

[0146] Referring to FIG. 23B, the printer output and decoding process will be explained. As shown in FIG. 23B, when the image stored in the form of codes using a page of image memory was decoded and outputted on the printer, the printer output was started after the completion of the decoding process for a page. After the printer output of the page of image finished, the decoding process of the next page was started.

[0147] Specifically, since the printer output and the decoding process were performed alternately, the decoding process was stopped during the printer output, whereas the printer output was stopped during the decoding process. This produced a dead time Tp during which printer output was not effected at all and a dead time Tu during which the decoding process was not effected at all, degrading the performance of the system.

[0148] With the present invention, to make the above-described dead times Td, Tc, Tp, and Tu as shorter as possible, the coding process and decoding process are started earlier. Such advance start can be controlled by software or hardware. The advance start of the coding and decoding processes by software control will be explained below.

[0149] First, the scanner input and coding process according to the present invention will be explained. With the invention, before a page of image data inputted from the scanner 13 have been all stored in the page memory 28, the coding process is started, thereby shortening the total processing time from the start of the scanner input of a page of image to the completion of the coding process.

[0150] To start the coding process earlier as shown in FIG. 24A, the reading of coded image data must be controlled so as not to pass the writing of image data from the scanner 13 into the page memory 28. Here, the page memory 28 is a memory capable of writing and reading at the same time. If reading passes writing, the totally irrelevant images left in the image memory will be coded.

[0151] The conditions for preventing such passing will be explained by reference to FIG. 25A. In general, the time required for the coding process varies with the feature of an image. The shortest time required to code a page of an image among all the images is determined to be the minimum coding time Dmin (in most cases, the coding of white paper corresponds to this case). To prevent the coding process from passing the scanner input, the coding process is started at a point in time later than the scanner input end time Te minus the minimum coding time Dmin.

[0152] This prevents the coding process from ending before the scanner 13 has ended the input even if the

coding process time is the minimum coding time Dmin. Therefore, it is possible to make the total processing time shorter than in a conventional sequential process by the minimum coding processing time Dmin. The scanner input of a second page is started after the coding process of the first page has ended. This is because the time required for each page to be coded is unknown and varies from page to page.

[0153] A first approach of preventing the coding process from passing the scanner input using software according to the above reasoning will be explained by reference to the flowchart of FIG. 26. In the flowchart of FIG. 26, the start timing of the coding process is determined by monitoring the number of words transferred from the scanner 13 to the page memory 28.

[0154] First, the minimum coding time for each image size and orientation (lengthways or widthways) of the manuscript, and the number (Ns) of words transferred from the scanner in a time interval between the scanner input start and the scanner input end time minus the minimum coding time are calculated in advance.

[0155] Then, as shown in FIG. 26, the reading of image data by the scanner 13 is started (step S1). Then, the number of words transferred from the scanner counted at the scanner-transferred-word-number counter 932 (see FIG. 20) is read (step S2) and it is judged whether or not the count has exceeded the number (Ns) of words transferred from the scanner (step S3). In the judgment at step S3, if the result is YES, that is, if the count has exceeded the number (Ns) of words transferred from the scanner, the coding process will be started (step S4).

[0156] Then, it is judged whether or not the coding process of a page has finished (step S5). In the judgment at step S5, if the result is YES, it will be judged whether or not any subsequent manuscript is present (step S6).

[0157] In the judgment at step S6, if the result is YES, control will return to step S1, where the scanner 13 will be started to read the next manuscript and load the image data into the page memory 28. In this way, the coded image data is stored in another area (code memory) in the page memory 28.

[0158] Now, a second approach of preventing the coding process from passing the scanner input using software will be explained by reference to FIG. 25A and the flowchart of FIG. 27. In the flowchart of FIG. 27, the start timing of the process of coding the scanner image data stored in the page memory is determined from the time at which the scanner started to operate. First, the minimum coding time Dmin for each image size and orientation (lengthways or widthways) of the manuscript, and the time Toffset (coding start offset time) from the scanner input start time to the scanner input end time Te minus the minimum coding time Dmin are calculated in advance.

[0159] The coding start offset time Toffset is set in the down counter 904 (FIG. 17) of the timer 10 (step S11). Then, the timer 10 is started and at the same time, the image input process by the scanner 16 is started (steps S12, S13). The coding start offset time Toffset set in the down counter 904 is counted down in response to the frequency-divided clock. Then, after the coding start offset time Toffset has elapsed since the start of the scanner input, the timer 10 outputs an interrupt signal to the system CPU 11. The system CPU 11 judges whether or not any interrupt signal has occurred (step S14). In the judgment at step S14, if the result is YES, the coding process will be started under the control of the system CPU 11.

[0160] Then, it is judged whether or not the coding process of a page has been completed (step S16). In the judgment at step S5, if the result is YES, it will be judged whether or not any subsequent manuscript is present (step S17).

[0161] In the judgment at step S17, if the result is YES, control will return to step S1, where the scanner 13 will be started to read the next manuscript and load the image data into the page memory 28. In this way, the coded image data is stored in another area (code memory) in the page memory 28.

[0162] Now, the printer output and decoding process according to the present invention will be described. In the invention, the total processing time from the start of the decoding process to the completion of the print output is shortened by starting the decoding process of the next page in the course of outputting a page of the coded image data stored in the page memory 28.

[0163] To start the decoding process earlier, the writing of decoded image data must be controlled so as not to pass the reading of image data from the page memory 28 onto the printer memory 15 as shown in FIG. 24B.

[0164] If reading passes writing, this will permit the decoded image data of the next page to be overwritten over the image data that has not been read yet, with the result that the image data to be outputted will be lost.

[0165] The conditions for preventing such passing will be explained by reference to FIG. 25B. In general, the time required for the decoding process varies with the feature of an image. The shortest time required to decode a page of an image among all the images is determined to be the minimum decoding time Pmin (in most cases, the decoding of white paper corresponds to this case). To prevent the decoding process from passing the printer output, the decoding process is started at a point in time later than the printer output end time To minus the minimum decoding time Pmin.

[0166] This prevent the decoding process from ending before the printer has ended the output even if the decoding process time is the minimum coding time Pmin. Therefore, it is possible to make the total processing time shorter than in a conventional sequential process by the minimum decoding processing time Pmin.

[0167] A first approach of preventing the decoding process from passing the printer output using software according to the above reasoning will be explained by

reference to the flowchart of FIG. 28. In the flowchart of FIG. 28, the start timing of the decoding process is determined by monitoring the number of words transferred to the printer.

[0168] First, the minimum decoding time Pmin for each image size and orientation (lengthways or widthways) of the manuscript, and the number (Np) of words transferred to the printer in a time interval between the printer output start and the printer output end time To minus the minimum decoding time Pmin are calculated in advance.

[0169] As shown in FIG. 28, the compression/expansion circuit 211 is caused to start decoding the first page (step S21). Then, it is judged whether or not the decoding of a page of coded images stored in the code area of the page memory 28 has been completed (step S22). If it is judged that the decoding has been completed, the printer will be started (step S23).

[0170] Then, it is judged whether or not the code area of the page memory 28 has any code in it (step S24). In the judgment at step S24, if the result is NO, the process will be terminated because there is no page to be decoded.

[0171] On the other hand, in the judgment at step S24, if the result is YES, the printer transfer word number counter 932 is read at regular intervals (step S25).

[0172] Then it is judged whether or not the number of words transferred to the printer counted at the printer transfer word number counter 932 has exceeded Np (step S26).

[0173] In the judgment at step S26, if the result is YES, control will return to step S21, where the decoding process of the next page stored in the code area of the page memory 28 will be started. After the decoding process of the next page has finished, the next page is printed out on the printer. This is because the time required to decode each page is unknown and varies from page to page.

[0174] A second method of preventing the decoding process from passing the printer output using software will be explained by reference to FIG. 25B and the flowchart of FIG. 29. In the flowchart of FIG. 29, the start timing of the decoding process at the compression/expansion circuit 211 is determined from the time at which the printer 15 started printing. First, as shown in FIG. 25B, the minimum decoding time Pmin for each image size and orientation (lengthways or widthways) of the manuscript, and the time Toffset (decoding start offset time) from the printer output start time To to the printer output end time minus the minimum decoding time Pmin are calculated in advance.

[0175] First, the decoding of the first page of codes stored by the compression/expansion circuit 211 in the code area of the page memory 28 is started (step S31). Then, it is judged whether or not the decoding of a page has been completed (step S32). In the judgment at step S32, if the result is YES, the decoding start offset time Toffset will be set in the down counter 904 of the timer 10 (step S33). Then, the timer 10 and printer 15 are caused to start operation (step S34, S35).

[0176] Then, it is judge whether or not the code area of the page memory 28 has another page to be decoded (step S36). If it is judged that there is no page to be decoded, the process will be terminated. The coding start offset time Toffset set in the down counter 904 is counted down in response to the frequency-divided clock. After the decoding start offset time Toffset has elapsed since the start of the printer output, the timer 10 outputs an interrupt signal to the system CPU 11. The system CPU 11 judges whether or not any interrupt signal has occurred (step S37).

[0177] In the judgment at step S37, if the result is YES, the decoding process of the next page will be started under the control of the system CPU 11 (step S31).

[0178] The above explanation is about the advance start of the coding and decoding processes by software control. Hereinafter, the passing prevention of the coding and decoding processes by hardware control will be explained.

[0179] First, the scanner input and coding process according to the present invention will be explained by reference to FIG. 30A. The scanner and the coding process are started at the same time and the coding process is controlled by hardware control so that the reading of the coded image data may not pass the writing of the image data from the scanner 13 into the image memory.

[0180] If the coding process is faster than the scanner input speed, the coding process will always keep up with the scanner input, enabling the coding process to end at the same time that the scanner input has finished.

[0181] First, the coding process will be described by reference to the flowchart of FIG. 31. FIFO control is enabled (step S41). Then, the input of the manuscript from the scanner 13 to the page memory 28 is started (step S42) and the coding into the code area of the page memory 28 is started (step S43).

[0182] Then, it is judged whether or not the coding of a page of data stored in the page memory 28 has been completed (step S44). In the judgment at step S44, if the result is YES, it will be judged whether or not any manuscript that follows is present (step S53). In the judgment at step S45, if the result is YES, the processes at steps S42 and S43 will be repeated. The series of processes is repeated as many times as the number of manuscripts to be stacked.

[0183] Next, a first method of preventing the coding process from passing the scanner input using hardware will be explained. The address in the page memory 28 in which the image data is written from the scanner 13 is compared with the address in the image memory from which the image data is read out for coding and the coding process is controlled.

[0184] The writing and reading of the data into and from the image memory are performed on one-dimensionally consecutive physical addresses in the image memory. The address in which the scanner input is writ-

ten is compared with the address from which the image is read out for coding. If they are equal, the image reading for coding will be inhibited, thereby preventing the coding from passing.

[0185] The fact that those two addresses are equal can be known from the empty signals (see FIG. 12) at the FIFO address generators 635, 636. By inputting the empty signal to the FIFO mask in the coding process channel of image bus mediation control 741, the coding process can be prevented by the empty signals from the FIFO address generators.

[0186] Hereinafter, a detailed explanation of FIFO control in coding will be given with reference to FIGS. 33A to 33D. FIGS. 33A to 33D show the state of the FIFO area. Because in the initial state shown in FIG. 33A, the scanner 13 has inputted nothing, there is no image data that can be read in the FIFO area and the FIFO status is empty, preventing the coded image data from being read.

[0187] Then, as shown in FIG. 33B, once the scanner input of the first page and the coding of the first page have been started, the image data is written from the scanner 13 into the FIFO area, which cancels the empty state of the FIFO status, allowing the image data to be read out for coding. The read-out image data is coded and written into the code area of the page memory 28.

[0188] Then, as shown in FIG. 33C, during the scanner input of the first page and the coding of the first page, if the reading of the image data for coding is faster than the speed of the scanner input, the unread image data will run out, making the FIFO status empty and preventing the reading of the image data for coding. Then, if new image data is inputted from the scanner, the empty state will be canceled and the image data for coding will be read out. This will be repeated.

[0189] As shown in FIG. 33D, once the input of a page of images has been completed, the coding of a page of images is terminated at the time when all the image data for coding has disappeared from the FIFO area.

[0190] Now, a second method of preventing the coding process from passing the scanner input using hardware will be explained. With the second method, the number of words of image data transferred from the scanner 13 and written into the page memory 28 is compared with the number of words of coded image data read and transferred from the image memory. If they are equal, the reading of the coded image will be inhibited, thereby preventing the coding process from passing.

[0191] The fact that the former number of words transferred has become equal to the latter can be known from the fact that the output signal of the number-of-transfers comparator 933 (see FIG. 20) in the terminal counter 745 has become active. By inputting the output signal of the number-of-transfers comparator 933 to the FIFO mask in the coding process channel in image bus mediation control 741, the reading operation for coding can be inhibited.

[0192] Now, the printer output and decoding process according to the present invention will be explained by reference to FIG. 30B. The printer output and the decoding process are started at the same time and the decoding process is controlled by hardware control so that the reading of the image data from the image memory onto the printer may not pass the writing of the decoded image data.

[0193] If the decoding process is faster than the printer output speed, the decoding process will always keep up with the printer output, enabling the decoding process to end at the same time that the printer output has finished.

[0194] The decoding process will be described by reference to the flowchart of FIG. 32. First, FIFO control is enabled (step S51). Then, the decoding process of the first page is started (step S52). Then, it is judged whether or not the decoding of a page of data has been completed (step S53).

[0195] In the judgment at step S53, if the result is YES, the output to the printer 15 will be started (step S54).

[0196] Then, it is judged whether or not any page of codes that follows is present (step S55). In the judgment at step S55, if the result is YES, the decoding process of the page following that decoded at step S52 will be started.

[0197] Next, a first method of preventing the decoding process from passing the printer output using hardware will be explained. Basically, the address in the page memory 28 from which the image data is read onto the printer 15 is compared with the address in the image memory into which the decoded image data is written and the decoding process is controlled.

[0198] The writing and reading of the data into and from the image memory 28 are performed on one-dimensionally consecutive physical addresses in the image memory 28.

[0199] The address from which the output is read onto the printer 15 is compared with the address in which the decoded image is written. If they are equal, the reading of the decoded image will be inhibited, thereby preventing the decoding from passing. The fact that those addresses have become equal can be known from the full signals from the FIFO address generators 635, 636.

[0200] By inputting the full signal to the FIFO mask in the decoding process channel in image bus mediation control 741, the decoding process can be prevented by the full signal (see FIG. 12) from the FIFO address generator.

[0201] A detailed explanation of FIFO control during such decoding will be given by reference to FIGS. 34A to 34F. Because decoding has not been effected in the initial state of FIG. 34A, there is no image data to be read and the FIFO status is empty and the printer 15 is out of operation.

[0202] Once the decoding of the first page has been started as shown in FIG. 34B, the decoded image data starts to be written into the FIFO area of the page memory 28.

[0203] Then, after the decoding of the first page has been completed as shown in FIG. 34C, the FIFO area has no empty area and the FIFO status becomes full, which prevents the coded image data from being written, stopping the decoding.

[0204] Next, as shown in FIG. 34D, the first page of decoded image data is outputted onto the printer 15 and at the same time, the decoding of the second page is started. When the output to the printer 15 is started, an empty area appears in the FIFO area, canceling the full status of FIFO. The writing of the second page of decoded image data is continued until the empty area has run out. Then, as shown in FIG. 34E, after the output of the first page onto the printer 15 has finished, the printer is stopped, and the FIFO area is filled with the second page of decoded image data, which makes the FIFO status full, terminating the decoding of the second page.

[0205] Then, as shown in FIG. 34F, the output of the second page onto the printer 15 and the decoding of the third page are started.

[0206] From this time on, the operation of performing the printer output and the decoding of the following page is repeated.

[0207] Now, a second method of preventing the decoding process from passing the printer output using hardware will be explained. With the second method, the number of words of image data read and transferred from the page memory 28 onto the printer 15 is compared with the number of words of decoded image data written into the page memory 28. If they are equal, the decoding process will be inhibited, thereby preventing the decoding process from passing. The fact that the former number of words transferred has become equal to the latter can be known from the fact that the output signal of the number-of-transfers comparator 933 (see FIG. 20) in the terminal counter 745 has become active. By inputting the output signal of the number-of-transfers comparator 933 to the FIFO mask in the decoding process channel in image bus mediation control 741, the decoding operation can be inhibited.

[0208] In the embodiment, the writing of the image data read by the scanner 13 into the page memory 28 and the coding of the image data and the decoding and printing of the coded data in the page memory 28 have been explained separately. If two pages of the page memory 28 are provided, the total processing time can be made shorter as much as the sum of the minimum coding time Dmin and the minimum decoding time Pmin by performing the writing of the image data read by the scanner 13 into the page memory 28 and the coding of the image data and the decoding and printing of the coded data in the page memory 28 at the same time (that is, performing the operation of FIG. 24A and that of FIG. 24B at the same time).

[0209] As explained in detail, with the present invention, the writing of image data from the scanner into the image memory, the coding of the image data read from the image memory, the decoding from the code memory to the image memory, and the image formation from the decoded image data read from the image memory are caused to be in progress simultaneously. This makes it possible to provide an image forming apparatus capable of shortening the time required for a series of image forming processes without increasing the capacity of the image memory, the series of image forming processes including the reading of image data into the image memory, the coding of the image data, the decoding of the coded data, and the image formation from the decoded image data read from the image memory.

Claims

1. An image forming apparatus comprising:

    image data producing means (13) for producing image data of an image on a page at a constant speed;

        an image memory (28) for storing image data of an image on at least one page;
        a code memory for storing code data of the image on said at least one page;
        image data writing means (21) for writing the image data produced by the image data producing means (13) in the image memory (28); and
        coding means (211) for reading the image data written by the image data writing means (21) from the image memory (28), coding the read image data to decrease a data amount thereof, thereby obtaining code data, and then writing the code data in the code memory, wherein
        the image forming apparatus further comprises coding control means (21) for controlling, when the coding means (211) reads the image data from the image memory (28) at a higher speed than a speed at which the image data writing means (21) writes the image data in the image memory (28), an image data reading operation of the coding means (211) such that the coding control means (21) makes the coding means (211) start a coding operation after the time which is earlier, by a minimum time period (Dmin) required for coding image data of one page, than the time (Te) at which the image data writing means (21) completes writing of the image data of one page.

2. An image forming apparatus according to claim 1, **characterized in that** the coding control means (21) includes written image data item counting means (932) for counting image data items writ-

ten by the image data writing means (21) in the image memory (28), and makes the coding operation start when the number of the image data items counted by the written image data items counting means (932) reaches a predetermined number.

3. An image forming apparatus according to claim 1,
characterized in that the coding control means (21) includes elapsed time counting means (904) for performing a counting operation from the time at which the image data writing means (21) starts to write the image data, thereby counting an elapsed time period, and makes the coding operation start when the number counted by the elapsed time counting means (904) reaches a predetermined number.

4. An image forming apparatus according to any of claims 1 to 3,
characterized in that the coding control means (21) includes memory address comparing means (635, 636) for comparing a memory write address of the image memory (28), which is selected by the image data writing means (21), with a memory read address of the image memory (28), which is selected by the coding means (211) and the coding control means (21) controls the image data reading operation of the coding means (211) such that the numeral of the memory read address is less than or equal to the numeral of the memory write address, on the basis of a result of comparison performed by the memory address comparing means (635, 636).

5. An image forming apparatus according to any of claims 1 to 3,
characterized in that: the coding control means (21) comprises

(i) written image data item counting means (932) for counting image data items written by the image data writing means (21) in the image memory (28),
(ii) read image data item counting means (932) for counting image data items read by the coding means (211) from the image memory (28), and
(iii) count number comparing means (933) for comparing the number of the written image data items counted by the written image data number counting means (932) and the number of the read image data items counted by the read image data number counting means (932); and wherein
the coding control means (21) controls the image data reading operation of the coding means (211) such that the number of the read image data items does not exceed the number of the written image data items, on the basis of a result of comparison performed by the count number comparing means (933).

6. An image forming apparatus accoring to any of claims 1 to 5,
characterized in that the coding control means (21) are adapted to control the image data reading operation of the coding means (211) such that a data amount of the image data read by the coding means (211) does not exceed a data amount of the image data written by the image data writing means (21) in the image memory (28).

7. An image forming apparatus comprising:

a code memory for storing code data of an image on a page or of images on pages in compressed form;
an image memory (28) for storing image data of the image on the page or of the images on the pages;
decoding means (211) for reading the image data from the code memory, decoding the read image data, and then writing the decoded image data in the image memory (28);
image data reading means (21) for reading the image data decoded by the decoding means (211) from the image memory (28) at a constant speed; and
printing/outputting means (9) for printing and outputting the image data of the image on the page, which is read by the image data reading means (21) from the image memory (28), wherein
the image forming apparatus further comprises decoding control means (21) for controlling, when the image data decoding means (211) writes the image data in the image memory (28) at a higher speed than the speed at which the image data reading means (21) reads the image data of the image on a current page from the image memory (28), an image data writing operation of the decoding means (211) in such a manner as to prevent the decoding means (211) from writing decoded image data of an image on a subsequent page onto that area of the current page, image data of which is not read by the image data reading means (21) from the image memory (28); and wherein
the decoding controlling means (21) makes the decoding means (211) start a decoding operation after the time which is earlier, by a minimum time period (Pmin) required for decoding the image data of the image on the page, than the time (To) at which the printing/outputting means (9) completes outputting of the image data of the image on the page.

8. An image forming apparatus according to claim 7, **characterized in that** the decoding control means (21) includes written image data item counting means (932) for counting the image data items read by the image data reading means (21) from the image memory (28), and makes the decoding operation start when the number of the image data items counted by the written image data item counting means (932) reaches a predetermined number.

9. An image forming apparatus according to claim 7, **characterized in that** the decoding control means (21) includes elapsed time counting means (904) for performing a counting operation from the time at which the image data reading means (21) starts to read the image data, thereby counting an elapsed time period, and makes the decoding operation start when the number counted by the elapsed time counting means (904) reaches a predetermined number.

10. An image forming apparatus according to any of claims 7 to 9, **characterized in that** the decoding control means (21) includes memory address comparing means (635, 636) for comparing a memory read address of the image memory (28), which is selected by the image data reading means (21), and a memory write address of the image memory (28), which is selected by the decoding means (211), and the decoding control means (21) controls the image data writing operation of the decoding means (211) such that the numeral of the memory write address is less than or equal to the numeral of the memory read address, on the basis of a result of comparison performed by the memory address comparing means (635, 636).

11. An image forming apparatus according to any of claims 7 to 9, **characterized in that:**

the decoding control means (21) comprises

(i) read image data item counting means (932) for counting the image data items on the page which is read by the image data reading means (21) from the image memory (28),
(ii) written image data item counting means (932) for counting the image data items on the subsequent page which is written by the decoding means (211) in the image memory (28), and
(iii) count number comparing means (933) for comparing the number of the written image data items counted by the written image data item counting means (932) and the number of the read image data items counted by the read image data item counting means (932); and wherein

the decoding control means (21) controls the image data reading operation of the decoding means (211) such that the number of the written image data items does not exceed the number of the read image data items

Patentansprüche

1. Bildausbildungsvorrichtung, die aufweist:

ein Bilddatenerzeugungsmittel (13) zum Erzeugen von Bilddaten eines Bildes auf einer Seite bei einer konstanten Geschwindigkeit;
einen Bildspeicher (28) zum Speichern von Bilddaten eines Bildes auf mindesens einer Seite;
einen Codespeicher zum Speichern von Codedaten des Bildes auf der mindestens einen Seite;
ein Bilddatenschreibmittel (21) zum Schreiben der Bilddaten, die durch das Bilddatenerzeugungsmittel (13) erzeugt worden sind, in den Bildspeicher (28); und
ein Codierungsmittel (211) zum Lesen der Bilddaten, die durch das Bilddatenschreibmittel (21) geschrieben worden sind, aus dem Bildspeicher (28), Codieren der gelesenen Bilddaten zum Vermindern einer Datenmenge derselben, wodurch Codedaten erhalten werden, und dann Schreiben der Codedaten in den Codespeicher, wobei
die Bildausbildungsvorrichtung weiter ein Codierungssteuermittel (21) zum Steuern, wenn das Codierungsmittel (211) die Bilddaten aus dem Bildspeicher (28) mit einer höheren Geschwindigkeit als eine Geschwindigkeit, mit der das Bilddatenschreibmittel (21) die Bilddaten in den Bildspeicher (28) schreibt, liest, eines Bilddatenlesebetriebes des Codierungsmittels (211) derart, daß das Codierungssteuermittel (21) das Codierungsmittel (211) zum Starten eines Codierungsbetriebes nach dem Zeitpunkt, der um einen Minimalzeitraum (Dmin), der zum Codieren von Bilddaten einer Seite benötigt wird, früher als der Zeitpunkt (Te), an dem das Bilddatenschreibmittel (21) das Schreiben der Bilddaten einer Seite vervollständigt, liegt, bringt.

2. Bildausbildungsvorrichtung nach Anspruch 1, **dadurch gekennzeichnet, daß** das Codierungssteuermittel (21) ein Zählmittel (932) für geschriebene Bilddatengegenstände zum Zählen von Bilddatengegenständen, die durch das Bilddaten-

schreibmittel (21) in den Bildspeicher (28) geschrieben worden sind, enthält und den Codierungsbetrieb zum Start bringt, wenn die Anzahl der durch das Zählmittel (932) für geschriebene Bilddatengegenstände gezählten Bilddatengegenstände eine vorbestimmte Anzahl erreicht.

3. Bildausbildungsvorrichtung nach Anspruch 1, **dadurch gekennzeichnet, daß** das Codierungssteuermittel (21) ein Zählmittel (904) für verstrichene Zeit zum Ausführen eines Zählbetriebes ab dem Zeitpunkt, an dem das Bilddatenschreibmittel (21) das Schreiben der Bilddaten beginnt, wodurch ein verstrichener Zeitraum gezählt wird, aufweist, und den Codierungsbetrieb zum Start bringt, wenn die durch das Zählmittel (904) für verstrichene Zeit gezählte Anzahl eine vorbestimmte Anzahl erreicht.

4. Bildausbildungsvorrichtung nach einem der Ansprüche 1 bis 3, **dadurch gekennzeichnet, daß** das Codierungssteuermittel (21) ein Speicheradreßvergleichsmittel (635, 636) zum Vergleichen einer Speicherschreibadresse des Bildspeichers (28), die durch das Bilddatenschreibmittel (21) ausgewählt ist, mit einer Speicherleseadresse des Bildspeichers (28), die durch das Codierungsmittel (211) ausgewählt ist, enthält und das Codierungssteuermittel (21) den Bilddatenlesebetrieb des Codierungsmittels (211) derart steuert, daß die Nummer der Speicherleseadresse kleiner als oder gleich zu der Nummer der Speicherschreibadresse ist, auf der Basis des Ergebnisses des Vergleichs, der durch das Speicheradreßvergleichsmittel (635, 636) ausgeführt wird.

5. Bildausbildungsvorrichtung nach einem der Ansprüche 1 bis 3, **dadurch gekennzeichnet, daß** das Codierungssteuermittel (21)

(i) ein Zählmittel (932) für geschriebene Bilddatengegenstände zum Zählen von Bilddatengegenständen, die durch das Bilddatenschreibmittel (21) in den Bildspeicher (28) geschrieben worden sind,
(ii) ein Zählmittel (932) für gelesene Bilddatengegenstände zum Zählen von Bilddatengegenständen, die durch das Codierungsmittel (211) aus dem Bildspeicher (28) gelesen worden sind, und
(iii) ein Vergleichsmittel (933) für gezählte Anzahlen zum Vergleichen der Anzahl der geschriebenen Bildgegenstände, die durch das Zählmittel (932) für eine geschriebene Bilddatenanzahl gezählt worden ist, und der Nummer der gelesenen Bilddatengegenstände, die durch das Zählmittel (932) für eine gelesene Bilddatenanzahl gezählt worden ist, aufweist,

und bei der

das Codierungssteuermittel (21) den Bilddatenlesebetrieb des Codierungsmittels (211) derart steuert, daß die Anzahl der gelesenen Bilddatengegenstände die Anzahl der geschriebenen Bilddatengegenstände nicht überschreitet, auf der Basis eines Ergebnisses des Vergleichs, der durch das Vergleichsmittel (933) für die gezählte Anzahl ausgeführt wird.

6. Bildausbildungsvorrichtung nach einem der Ansprüche 1 bis 5, **dadurch gekennzeichnet, daß** das Codierungssteuermittel (21) angepaßt ist zum Steuern des Bilddatenlesebetriebs des Codierungsmittels (211) derart, daß eine Datenmenge der durch das Codierungsmittel (211) gelesenen Bilddaten eine Datenmenge der durch das Bilddatenschreibmittel (21) in den Bildspeicher (28) geschriebenen Bilddaten nicht überschreitet.

7. Bildausbildungsvorrichtung, die aufweist:

einen Codespeicher zum Speichern von Codedaten eines Bildes auf einer Seite oder von Bildern auf Seiten in einer komprimierten Form;
einen Bildspeicher (28) zum Speichern von Bilddaten des Bildes auf der Seite oder der Bilder auf den Seiten;
ein Decodierungsmittel (211) zum Lesen der Bilddaten aus dem Codespeicher, Decodieren der gelesenen Bilddaten, und dann Schreiben der decodierten Bilddaten in den Bildspeicher (28);
ein Bilddatenlesemittel (21) zum Lesen der durch das Decodierungsmittel (211) decodierten Bilddaten aus dem Bildspeicher (28) bei einer konstanten Geschwindigkeit; und
ein Druck/Ausgabe-Mittel (9) zum Drucken und Ausgeben der Bilddaten des Bildes auf der Seite, die durch das Bilddatenlesemittel (211) aus dem Bildspeicher (28) gelesen werden, wobei die Bilddatenausbildungsvorrichtung weiter ein Decodierungssteuermittel (21) zum Steuern, wenn das Bilddatendecodierungsmittel (211) die Bilddaten in den Bildspeicher (28) mit einer höheren Geschwindigkeit als der Geschwindigkeit, mit der das Bilddatenlesemittel (21) die Bilddaten des Bildes über eine momentane Seite aus dem Bildspeicher (28) liest, schreibt, eines Bilddatenschreibbetriebs des Decodierungsmittels (211) in einer solchen Weise, daß das Decodierungsmittel (211) am Schreiben von decodierten Bilddaten eines Bildes auf einer nachfolgenden Seite auf den Bereich der momentanen Seite, deren Bilddaten durch das Bilddatenlesemittel (21) nicht aus dem Bild-

speicher (28) gelesen worden sind, hindert, und wobei
das Decodierungssteuermittel (21) das Decodierungsmittel (211) zum Starten eines Decodierungsbetriebes nach dem Zeitpunkt, der um einen minimalen Zeitraum (Pmin), der zum Decodieren der Bilddaten des Bildes auf der Seite benötigt wird, früher als der Zeitpunkt (T_0), an dem das Druck/Ausgabe-Mittel (9) das Ausgeben der Bilddaten des Bildes auf der Seite vervollständigt, liegt, bringt.

8. Bildausbildungsvorrichtung nach Anspruch 7, **dadurch gekennzeichnet, daß** das Decodierungssteuermittel (21) ein Zählmittel (932) für geschriebene Bilddatengegenstände zum Zählen der Bilddatengegenstände, die durch das Bilddatenlesemittel (21) aus dem Bildspeicher (28) gelesen worden sind, enthält und den Decodierungsbetrieb zum Starten bringt, wenn die Anzahl der durch das Zählmittel (932) für geschriebene Bilddatengegenstände gezählten Bilddatengegenstände eine vorbestimmte Anzahl erreicht.

9. Bildausbildungsvorrichtung nach Anspruch 7, **dadurch gekennzeichnet, daß** das Decodierungssteuermittel (21) ein Zählmittel (904) für verstrichene Zeit zum Ausführen eines Zählbetriebes von dem Zeitpunkt an, an dem das Bilddatenlesemittel (21) das Lesen der Bilddaten beginnt, wodurch ein verstrichener Zeitraum gezählt wird, enthält und den Decodierungsbetrieb zum Start bringt, wenn die durch das Zählmittel (904) für verstrichene Zeit gezählte Anzahl eine vorbestimmte Anzahl erreicht.

10. Bildausbildungsvorrichtung nach einem der Ansprüche 7 bis 9, **dadurch gekennzeichnet, daß** das Decodierungssteuermittel (21) ein Speicheradreßvergleichsmittel (635, 636) zum Vergleichen einer Speicherleseadresse des Bildspeichers (28), die durch das Bilddatenlesemittel (21) ausgewählt worden ist, und einer Speicherschreibadresse des Bildspeichers (28), die durch das Decodierungsmittel (211) ausgewählt worden ist, enthält und das Decodierungssteuermittel (21) den Bilddatenschreibbetrieb des Decodierungsmittels (211) derart steuert, daß die Nummer der Speicherschreibadresse kleiner als oder gleich zu der Nummer der Speicherleseadresse ist, auf der Basis eines Ergebnisses eines Vergleichs, der durch das Speicheradreßvergleichsmittel (635, 636) ausgeführt wird.

11. Bildausbildungsvorrichtung nach einem der Ansprüche 7 bis 9, **dadurch gekennzeichnet, daß** das Decodierungssteuermittel (21)

(i) ein Zählmittel (932) für gelesene Bilddatengegenstände zum Zählen der Bilddatengegenstände auf der Seite, die durch das Bilddatenlesemittel (21) aus dem Bildspeicher (28) gelesen wird,
(ii) ein Zählmittel (932) für geschriebene Bilddatengegenstände zum Zählen der Bilddatengegenstände auf der nachfolgenden Seite, die durch das Decodierungsmittel (211) in den Bildspeicher (28) geschrieben wird, und
(iii) ein Vergleichsmittel (933) für gezählte Zahlen zum Vergleichen der Anzahl der geschriebenen Bilddatengegenstände, die durch das Zählmittel (932) für geschriebene Bilddatengegenstände gezählt worden ist, und der Anzahl der gelesenen Bilddatengegenstände, die durch das Zählmittel (932) für gelesene Bilddatengegenstände gezählt worden ist,

aufweist, und bei der
das Decodierungssteuermittel (21) den Bilddatenlesebetrieb des Decodierungsmittels (211) derart steuert, daß die Anzahl der geschriebenen Bilddatengegenstände die Anzahl der gelesenen Bilddatengegenstände nicht überschreitet.

Revendications

1. Appareil de formation d'image comprenant :

un moyen de production de données d'image (13) pour produire des données d'image d'une image sur une page à une vitesse constante ;
une mémoire d'image (28) pour stocker des données d'image d'une image sur au moins une page ;
une mémoire de code pour stocker des données de code de l'image sur ladite au moins une page ;
un moyen d'écriture des données d'images (21) pour écrire les données d'image produites par le moyen de production de données (13) dans la mémoire d'image (28) ; et
un moyen de codage (211) pour lire les données d'image écrites par le moyen d'écriture des données d'images (21) à partir de la mémoire d'image (28), pour coder les données d'image lues pour diminuer la quantité de données associées, obtenant ainsi des données de code, et puis pour écrire les données de code dans la mémoire de code où
l'appareil de formation d'image comprend en outre un moyen de commande de code (21) pour commander, lorsque le moyen de codage (211) lit les données d'image à partir de la mémoire d'image (28) à une vitesse supérieure à une vitesse à laquelle le moyen d'écriture des

données d'images (21) écrit les données d'image dans la mémoire d'image (28), une opération de lecture de données d'image du moyen de codage (211) pour que le moyen de commande de codage (21) fasse que le moyen de codage (211) commence une opération de codage après un temps qui est plus tôt, d'une période de temps minimum (Dmin) nécessaire pour le codage des données d'image d'une page, que le temps (Te) auquel le moyen d'écriture des données d'images (21) termine l'écriture des données d'image d'une page.

2. Appareil de formation d'image selon la revendication 1,

caractérisé en ce que le moyen de commande de codage (21) comprend un moyen de comptage d'éléments de données d'image écrits (932) pour compter des éléments de données d'image écrits par le moyen d'écriture des données images (21) dans la mémoire d'image (28), et fasse que l'opération de comptage commence lorsque le nombre d'éléments de données d'image compté par le moyen de comptage d'éléments de données d'image écrits (932) atteigne un nombre prédéterminé.

3. Appareil de formation d'image selon la revendication 1,

caractérisé en ce que ledit moyen de commande de codage (21) comprend un moyen de comptage du temps écoulé (904) pour réaliser une opération de comptage à partir du temps auquel le moyen d'écriture des données images (21) commence à écrire les données d'image, comptant ainsi une période temps écoulé, et fasse que l'opération de codage commence lorsque le nombre compté par le moyen de comptage de temps écoulé (904) atteint un nombre prédéterminé.

4. Appareil de formation d'image selon l'une quelconque des revendications 1 à 3,

caractérisé en ce que le moyen de commande de codage (21) comprend un moyen de comparaison d'adresse de mémoire (635, 636) pour comparer une adresse d'écriture de mémoire d'une mémoire d'image (28), qui est sélectionnée par le moyen d'écriture des données images (21), avec une adresse de lecture de mémoire de la mémoire d'image (28) qui est sélectionnée par le moyen de codage (211) et le moyen de commande de codage (21) commande l'opération de lecture de données d'image du moyen de codage (211) pour que le numéro de l'adresse lue de mémoire soit inférieur ou égal au numéro de l'adresse d'écriture de mémoire, sur la base d'un résultat de comparaison réalisé par le moyen de comparaison d'adresse de mémoire (635, 636).

5. Appareil de formation d'image selon l'une quelconque des revendications 1 à 3, **caractérisé en ce que** le moyen de commande de codage (21) comprend :

(i) le moyen de comptage d'éléments de données d'image écrits (932) pour compter des éléments de données d'image écrits par le moyen d'écriture des données images (21) dans la mémoire d'image (28),
(ii) le moyen de comptage d'éléments de données d'image lus (932) pour compter des éléments de données d'image lus par le moyen de codage (211) à partir de la mémoire d'image (28) ; et
(iii) le moyen de comparaison de nombre de comptage (933) pour comparer le nombre d'éléments de données d'image écrits compté par le moyen de comptage du nombre de données d'image écrites (932) et le nombre d'éléments de données lues compté par le moyen de comptage de nombre de données d'image lues (932) ; et où

le moyen de commande de codage (21) commande l'opération de lecture de données d'image du moyen de codage (211) pour que le nombre d'éléments de données d'image lus n'excède pas le nombre d'éléments de données d'image écrits, sur la base d'un résultat de comparaison réalisé par le moyen de comparaison de nombre de comptage (933).

6. Appareil de formation d'image selon l'une quelconque des revendications 1 à 5,

caractérisé en ce que les moyens de commande de codage (21) sont adaptés pour commander l'opération de lecture de données d'image du moyen de codage (211) pour que la quantité de données des données d'image lues par le moyen de codage (211) n'excède pas une quantité de données des données d'image écrites par le moyen d'écriture des données d'image (21) dans la mémoire d'image (28).

7. Appareil de formation d'image comprenant :

une mémoire de code pour stocker des données de code d'une image sur une page ou d'images sur des pages dans une forme compressée ;
une mémoire d'image (28) pour stocker des données d'image des images sur la page ou des images sur les pages ;
un moyen de décodage (211) pour lire les données d'image à partir de la mémoire de code, décodant les données d'image lues, et puis écrire des données d'image décodées dans la

mémoire d'image (28) ;
le moyen de lecture de données d'image (21) pour lire les données d'image décodées par le moyen de décodage (211) à partir de la mémoire d'image (28) à une vitesse constante ; et
un moyen d'écriture/sortie (9) pour imprimer et fournir les données d'image de l'image sur la page, qui est lue par le moyen de lecture de données d'image (21) à partir de la mémoire d'image (28) dans lequel :

l'appareil de formation d'image comprend en outre le moyen de commande de décodage (21) pour commander, lorsque le moyen décodage de données d'image (211) écrit des données d'image dans la mémoire d'image (28) à une vitesse supérieure à la vitesse à laquelle le moyen de lecture de données d'image (21) lit les données d'image de l'image sur une page actuelle à partir de la mémoire d'image (28), une opération d'écriture des données d'image du moyen de décodage (211) de manière à empêcher le moyen de décodage (211) d'écrire des données d'image décodées d'une image sur une page suivante sur cette zone de la page actuelle, dont les données d'image ne sont pas lues par le moyen de lecture de données d'image (21) à partir de la mémoire d'image (28) ; et où le moyen de commande de décodage (21) fait que le moyen de décodage (211) commence une opération de décodage après un moment qui est plus tôt, d'une période de temps minimum (Pmin) nécessaire pour décoder les données d'image de l'image sur la page, que le temps (To) auquel le moyen d'impression/sortie (9) termine la sortie des données d'image de l'image sur cette page.

8. Appareil de formation d'image selon la revendication 7,
caractérisé en ce que le moyen de commande de décodage (21) comprend un moyen de comptage d'éléments de données d'image écrits (932) pour compter des éléments de données d'image lus par le moyen de lecture de données d'image (21) à partir de la mémoire d'image (28), et fait que l'opération de décodage commence lorsque le nombre d'éléments de données d'image compté par le moyen de comptage d'éléments de données d'image écrits (932) atteint un nombre prédéterminé.

9. Appareil de formation d'image selon la revendication 7
caractérisé en ce que le moyen de commande de décodage (21) comprend un moyen de comptage de temps écoulé (904) pour réaliser une opération de comptage à partir du moment auquel le moyen de lecture de données d'image (21) commence à lire les données d'image, comptant ainsi une période de temps écoulé, et fait que l'opération de décodage commence lorsque le nombre compté par le moyen de comptage de temps écoulé (904) atteint un nombre prédéterminé.

10. Appareil de formation d'image selon l'une quelconque des revendications 7 à 9,
caractérisé en ce que le moyen de commande de codage (21) comprend un moyen de comparaison d'adresse de mémoire (635, 636) pour comparer une adresse de lecture de mémoire de la mémoire d'image (28) qui est sélectionnée par un moyen de lecture de données d'image (21), et une adresse d'écriture de mémoire de la mémoire d'image (28) qui est sélectionnée par le moyen de décodage (211), et le moyen de commande de décodage (21) commande l'opération d'écriture des données d'image du moyen de décodage (211) pour que le numéro de l'adresse d'écriture de mémoire soit inférieur ou égal au numéro de l'adresse de lecture de mémoire, sur la base de résultat de comparaison réalisé par le moyen de comparaison d'adresse de mémoire (635, 636).

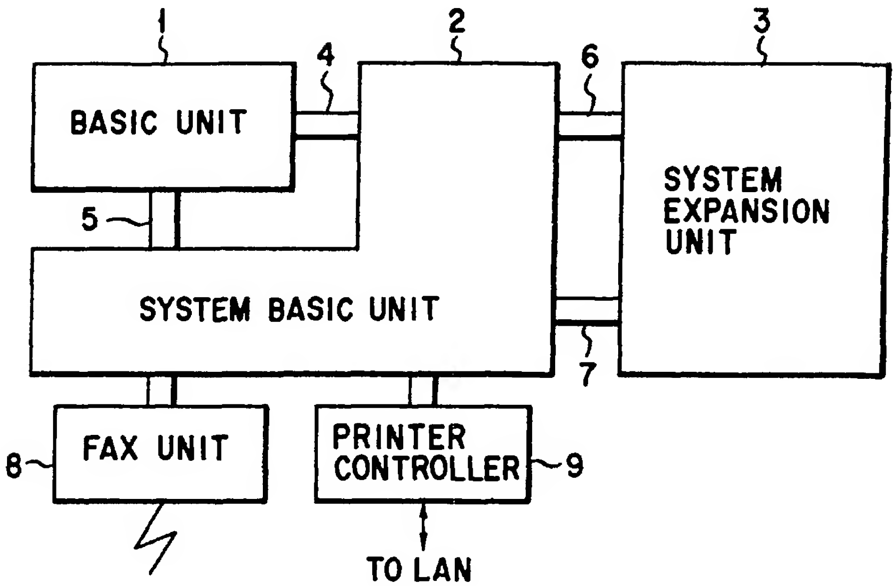
11. Appareil de formation d'image selon l'une quelconque des revendications 7 à 9, **caractérisé en ce que** :

le moyen de commande de codage (21) comprend :

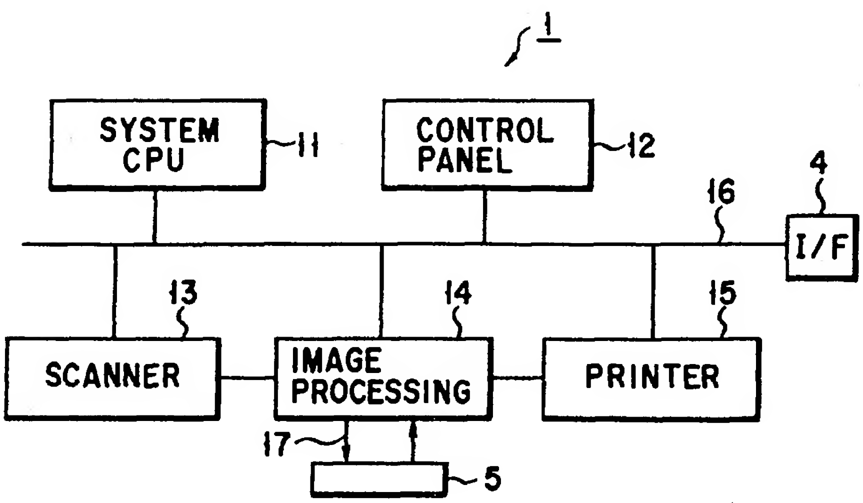
(i) un moyen de comptage d'éléments de données d'image de lecture (932) pour compter les éléments de données d'image sur la page qui est lue par le moyen de lecture de données d'images (21) à partir de la mémoire d'image (28),
(ii) un moyen de comptage d'éléments de données d'image écrits (932) pour compter les éléments de données d'image sur la page suivante qui est écrite par le moyen de décodage (211) dans la mémoire d'image (28), et
(iii) le moyen de comparaison du nombre de comptage (933) pour comparer le nombre des éléments de données d'image écrits compté par le moyen de comptage d'éléments de données d'image écrits (932) et le nombre d'éléments de données d'image lus compté par le moyen de comptage d'éléments de données d'image lus (932) ; et où

le moyen de commande de décodage (21)

commande l'opération de lecture de données d'image du moyen de décodage (211) pour que le nombre d'éléments de données d'image écrits n'excède pas le nombre d'éléments de données d'image lus.


1
2
3
4
6
BASIC UNIT
SYSTEM
EXPANSION
UNIT
5
SYSTEM BASIC UNIT
7
FAX UNIT
8
PRINTER
CONTROLLER
9
TO LAN

F I G. 1


1
SYSTEM
CPU
11
CONTROL
PANEL
12
4
16
I/F
13
14
15
SCANNER
IMAGE
PROCESSING
PRINTER
17
5

F I G. 2

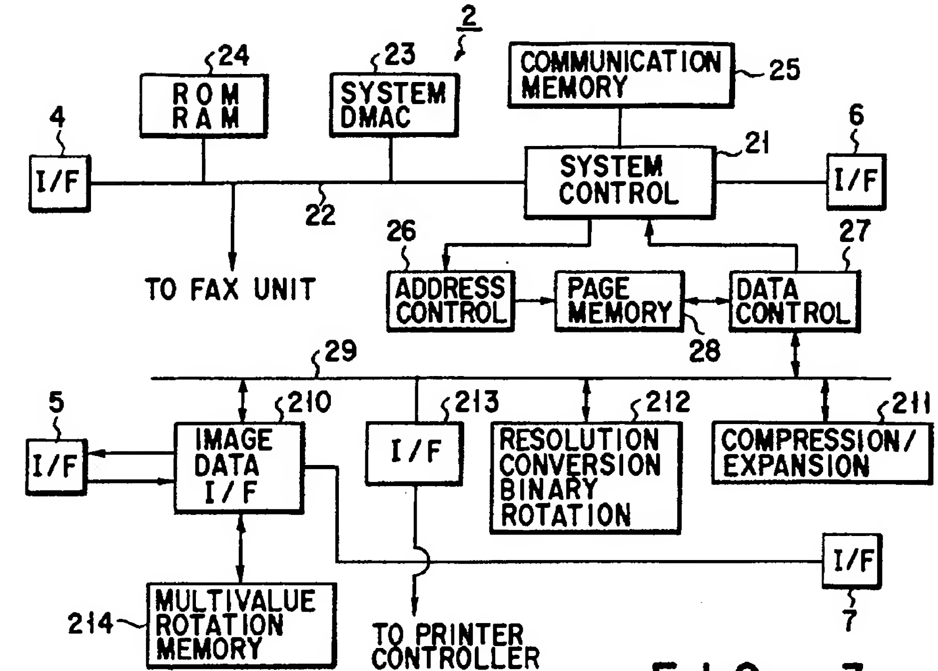

2
24
ROM
RAM
23
SYSTEM
DMAC
COMMUNICATION
MEMORY
25
4
I/F
21
SYSTEM
CONTROL
6
I/F
22
TO FAX UNIT
26
ADDRESS
CONTROL
PAGE
MEMORY
28
27
DATA
CONTROL
29
5
I/F
210
IMAGE
DATA
I/F
213
I/F
212
RESOLUTION
CONVERSION
BINARY
ROTATION
211
COMPRESSION/
EXPANSION
I/F
7
214
MULTIVALUE
ROTATION
MEMORY
TO PRINTER
CONTROLLER

FIG. 3

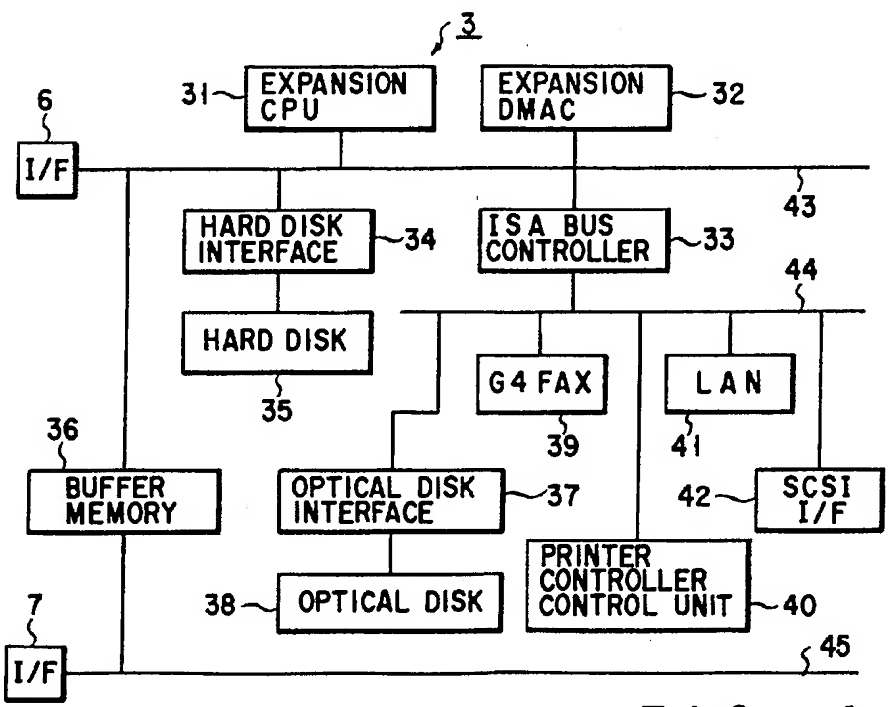
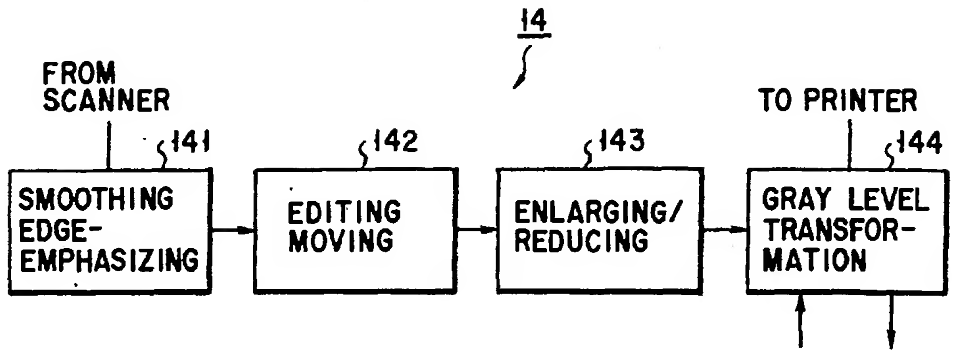
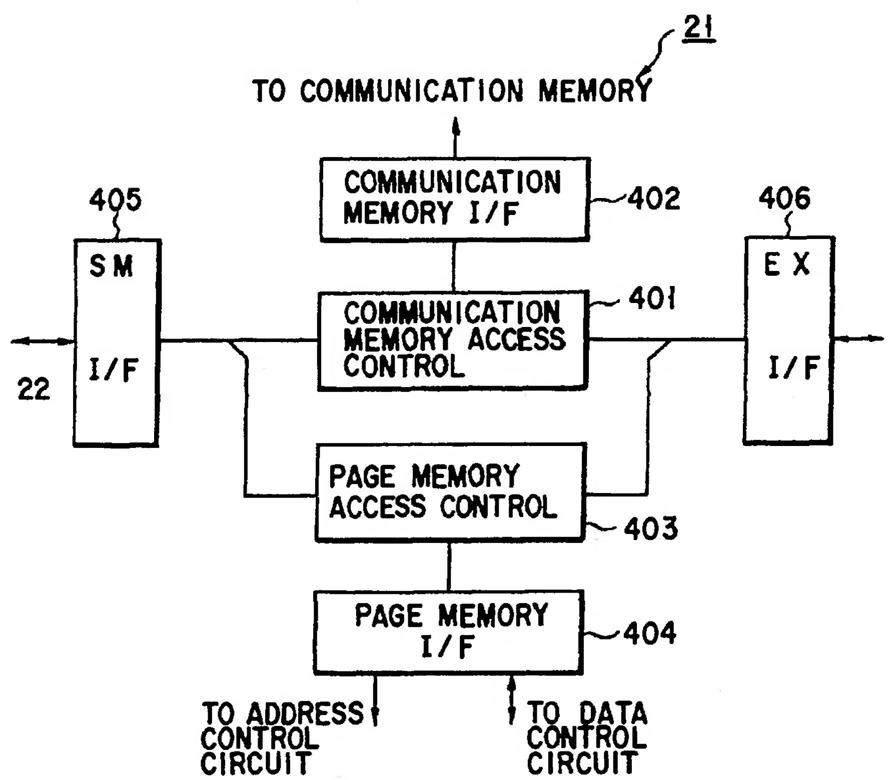

3
31
EXPANSION
CPU
EXPANSION
DMAC
32
6
I/F
43
HARD DISK
INTERFACE
34
ISA BUS
CONTROLLER
33
44
HARD DISK
35
G4 FAX
39
LAN
41
36
BUFFER
MEMORY
OPTICAL DISK
INTERFACE
37
42
SCSI
I/F
PRINTER
CONTROLLER
CONTROL UNIT
40
7
I/F
38
OPTICAL DISK
45

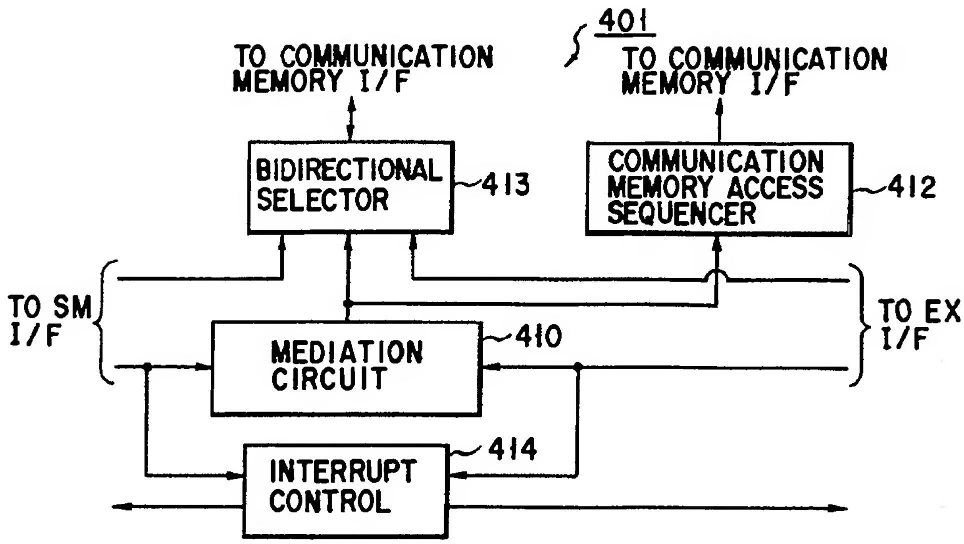
FIG. 4


14
FROM SCANNER
TO PRINTER
141
142
143
144
SMOOTHING EDGE-EMPHASIZING
EDITING MOVING
ENLARGING/ REDUCING
GRAY LEVEL TRANSFOR-MATION

F I G. 5

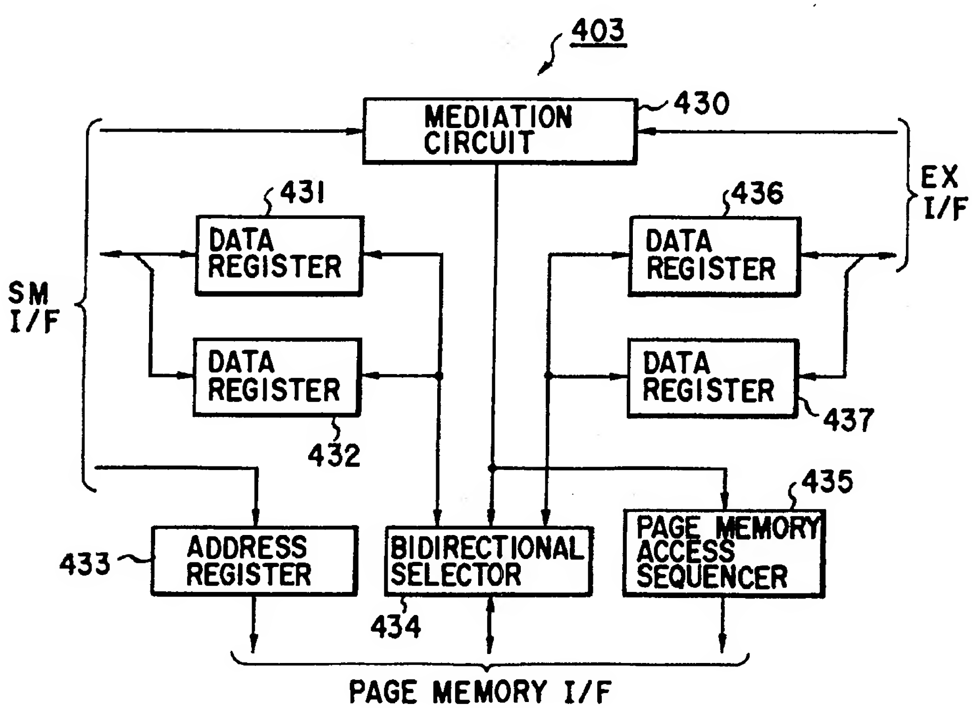

21
TO COMMUNICATION MEMORY
COMMUNICATION MEMORY I/F
402
405
406
S M
I/F
22
COMMUNICATION MEMORY ACCESS CONTROL
401
E X
I/F
PAGE MEMORY ACCESS CONTROL
403
PAGE MEMORY I/F
404
TO ADDRESS CONTROL CIRCUIT
TO DATA CONTROL CIRCUIT

F I G. 6



401
TO COMMUNICATION MEMORY I/F
TO COMMUNICATION MEMORY I/F
BIDIRECTIONAL SELECTOR
413
COMMUNICATION MEMORY ACCESS SEQUENCER
412
TO SM I/F
TO EX I/F
MEDIATION CIRCUIT
410
INTERRUPT CONTROL
414

F I G. 7



403
MEDIATION CIRCUIT
430
EX I/F
431
436
DATA REGISTER
DATA REGISTER
SM I/F
DATA REGISTER
DATA REGISTER
437
432
435
433
ADDRESS REGISTER
BIDIRECTIONAL SELECTOR
434
PAGE MEMORY ACCESS SEQUENCER
PAGE MEMORY I/F

F I G. 8

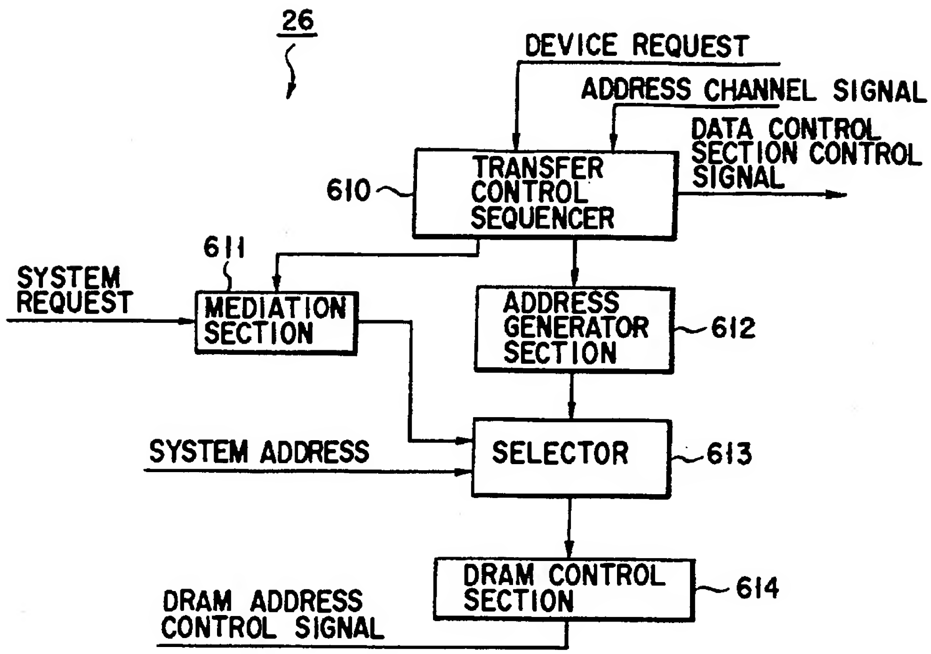

26
DEVICE REQUEST
ADDRESS CHANNEL SIGNAL
DATA CONTROL SECTION CONTROL SIGNAL
610
TRANSFER CONTROL SEQUENCER
611
SYSTEM REQUEST
MEDIATION SECTION
ADDRESS GENERATOR SECTION
612
SYSTEM ADDRESS
SELECTOR
613
DRAM CONTROL SECTION
614
DRAM ADDRESS CONTROL SIGNAL

FIG. 9

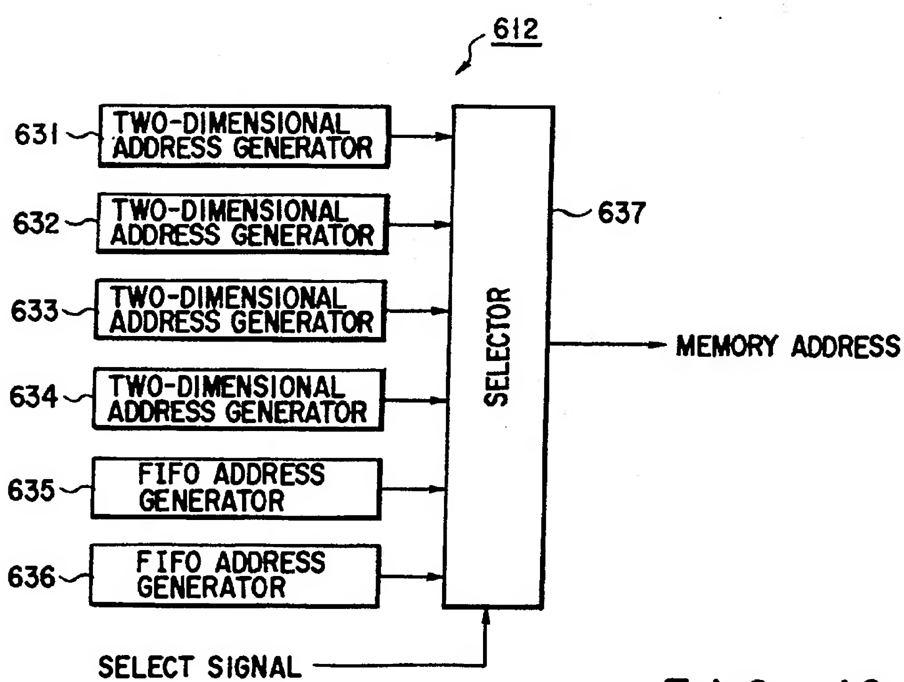

612
631
TWO-DIMENSIONAL ADDRESS GENERATOR
632
TWO-DIMENSIONAL ADDRESS GENERATOR
633
TWO-DIMENSIONAL ADDRESS GENERATOR
634
TWO-DIMENSIONAL ADDRESS GENERATOR
635
FIFO ADDRESS GENERATOR
636
FIFO ADDRESS GENERATOR
SELECTOR
637
MEMORY ADDRESS
SELECT SIGNAL

FIG. 10

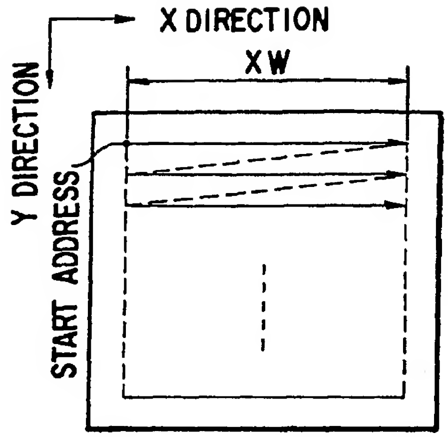


FIG. 11A

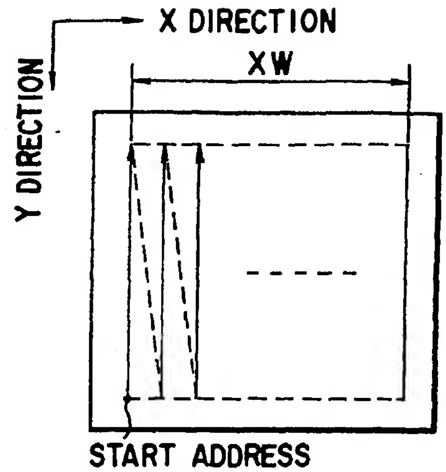


FIG. 11B

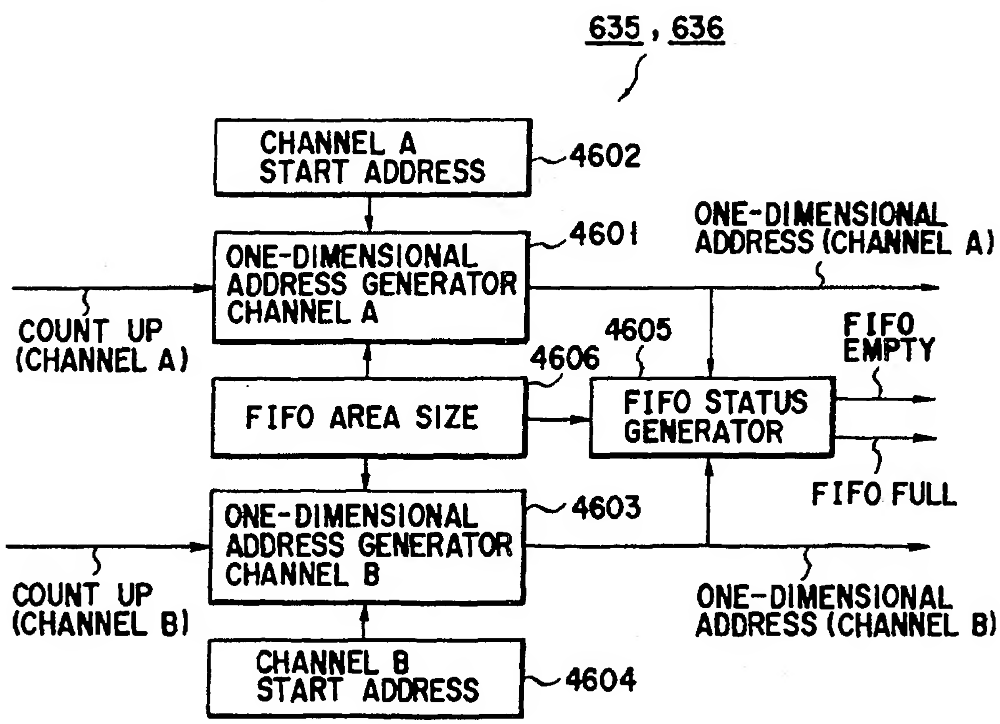


FIG. 12

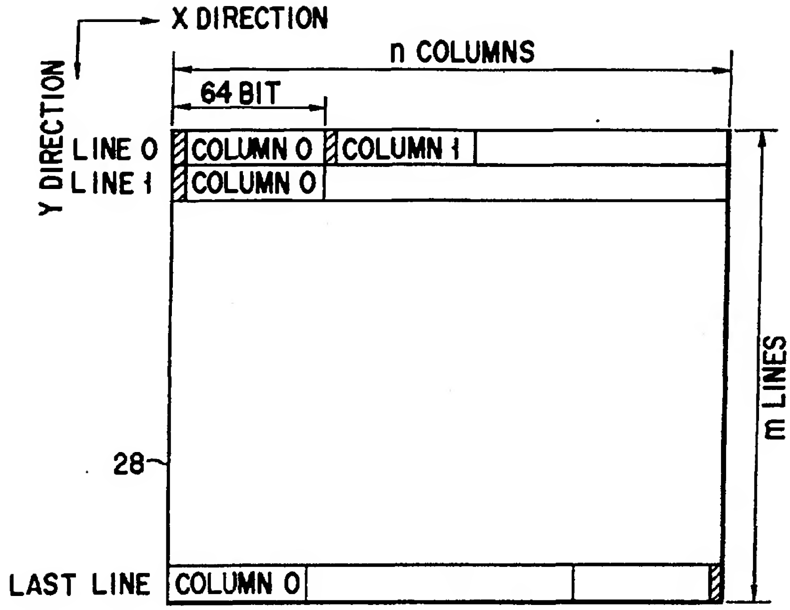

X DIRECTION
Y DIRECTION
n COLUMNS
64 BIT
LINE 0
LINE 1
COLUMN 0
COLUMN 1
COLUMN 0
m LINES
28
LAST LINE
COLUMN 0

FIG. 13

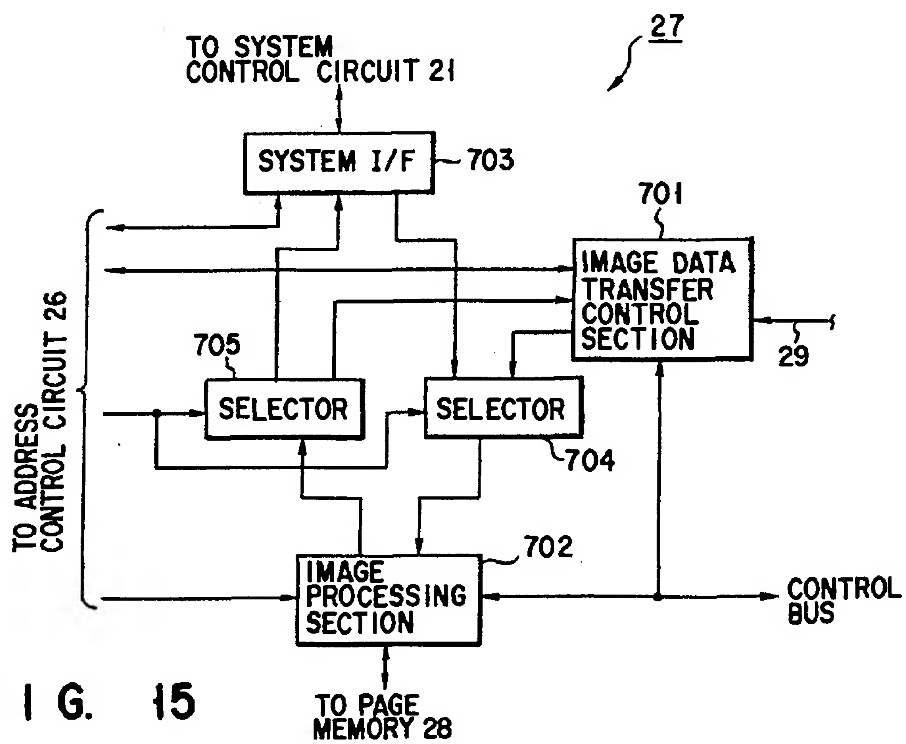

27
TO SYSTEM CONTROL CIRCUIT 21
SYSTEM I/F
703
701
IMAGE DATA TRANSFER CONTROL SECTION
29
705
SELECTOR
SELECTOR
704
TO ADDRESS CONTROL CIRCUIT 26
702
IMAGE PROCESSING SECTION
CONTROL BUS
TO PAGE MEMORY 28

FIG. 15

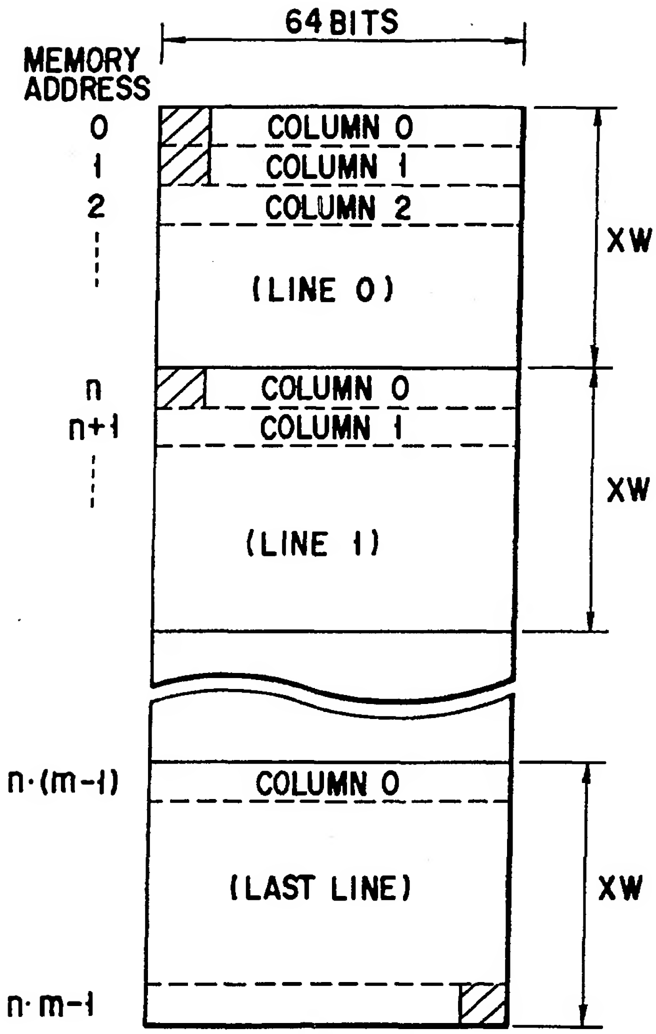
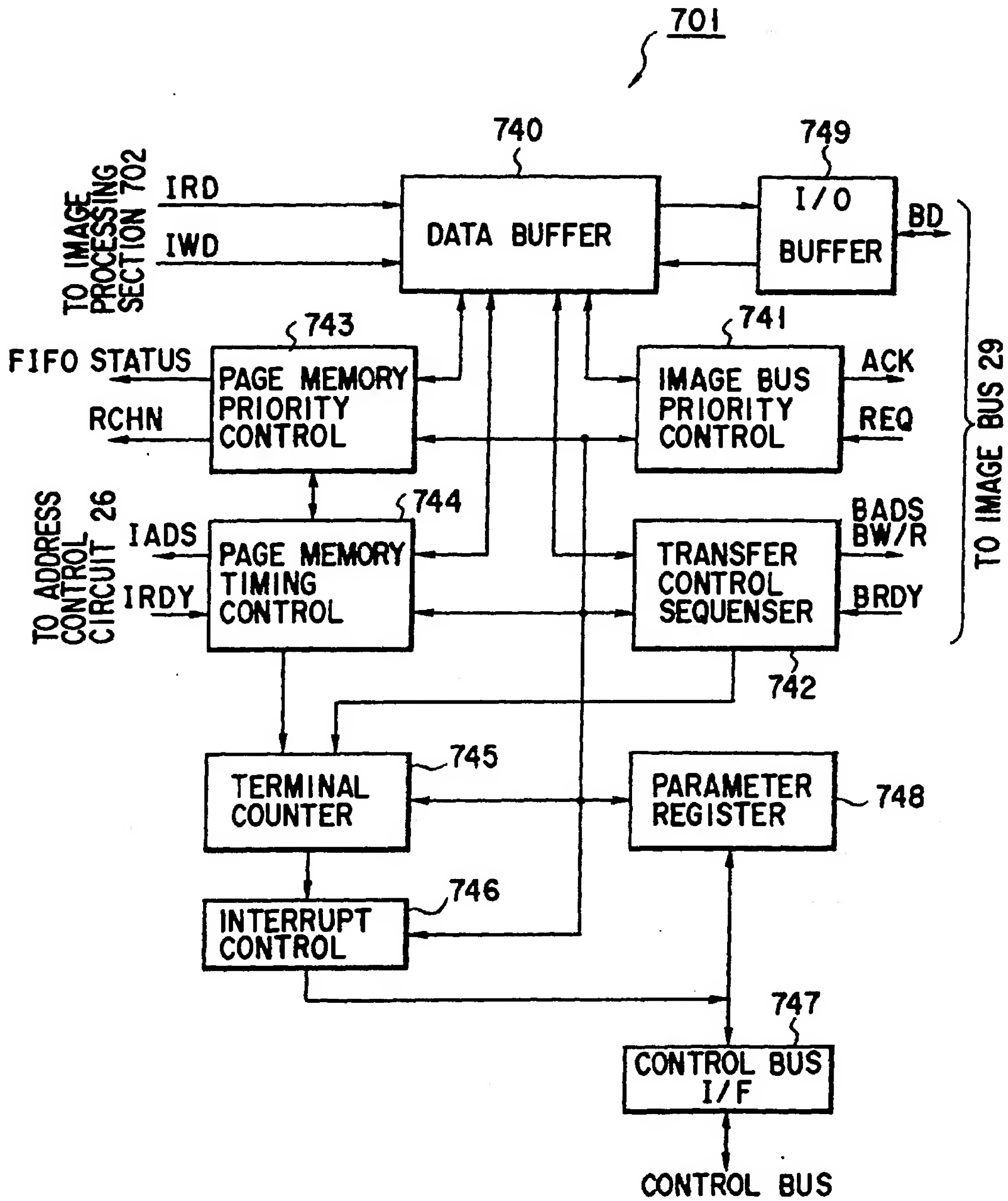
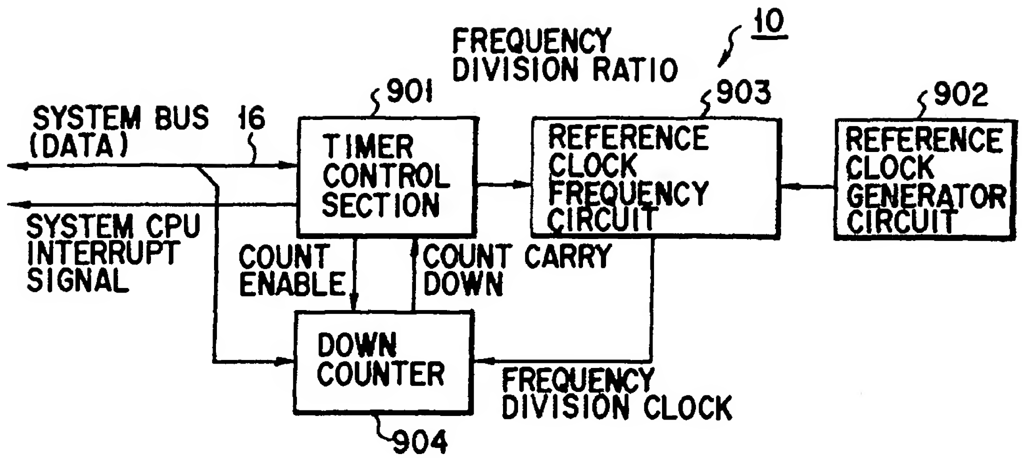

64 BITS
MEMORY ADDRESS
0
1
2
COLUMN 0
COLUMN 1
COLUMN 2
(LINE 0)
XW
n
n+1
COLUMN 0
COLUMN 1
(LINE 1)
XW
n·(m-1)
COLUMN 0
(LAST LINE)
XW
n·m-1

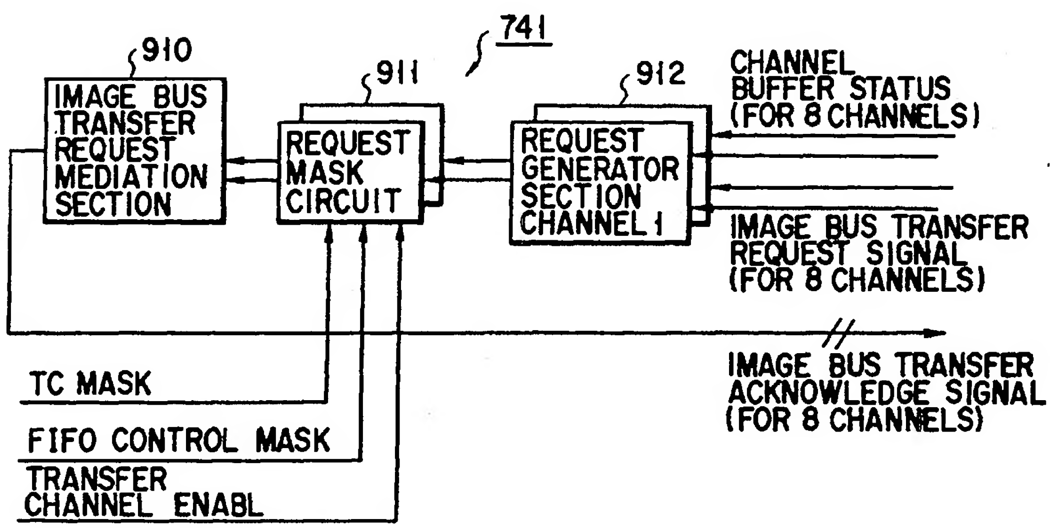
FIG. 14


701
740
749
TO IMAGE PROCESSING SECTION 702
IRD
IWD
DATA BUFFER
I/O BUFFER
BD
743
741
FIFO STATUS
RCHN
PAGE MEMORY PRIORITY CONTROL
IMAGE BUS PRIORITY CONTROL
ACK
REQ
TO IMAGE BUS 29
744
TO ADDRESS CONTROL CIRCUIT 26
IADS
IRDY
PAGE MEMORY TIMING CONTROL
TRANSFER CONTROL SEQUENSER
BADS
BW/R
BRDY
742
TERMINAL COUNTER
745
PARAMETER REGISTER
748
INTERRUPT CONTROL
746
747
CONTROL BUS I/F
CONTROL BUS

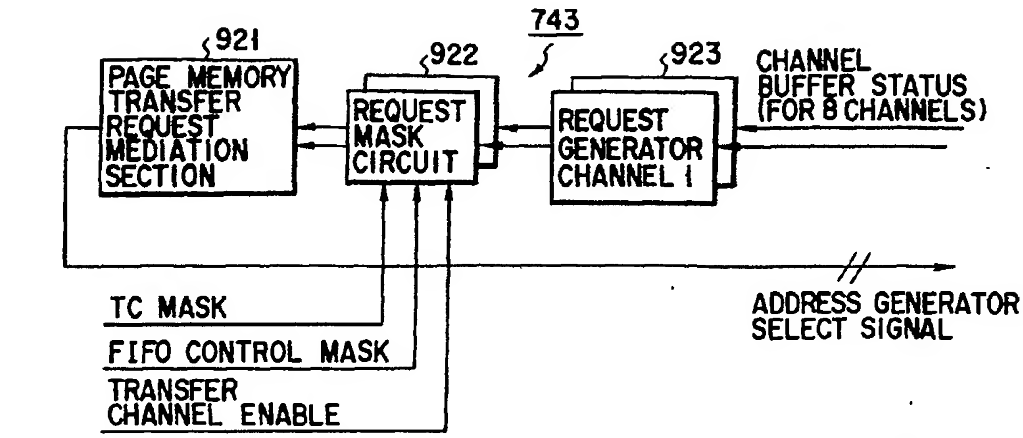
F I G. 16


FREQUENCY
DIVISION RATIO
10
901
903
902
SYSTEM BUS 16
(DATA)
TIMER
CONTROL
SECTION
REFERENCE
CLOCK
FREQUENCY
CIRCUIT
REFERENCE
CLOCK
GENERATOR
CIRCUIT
SYSTEM CPU
INTERRUPT
SIGNAL
COUNT
ENABLE
COUNT CARRY
DOWN
DOWN
COUNTER
FREQUENCY
DIVISION CLOCK
904

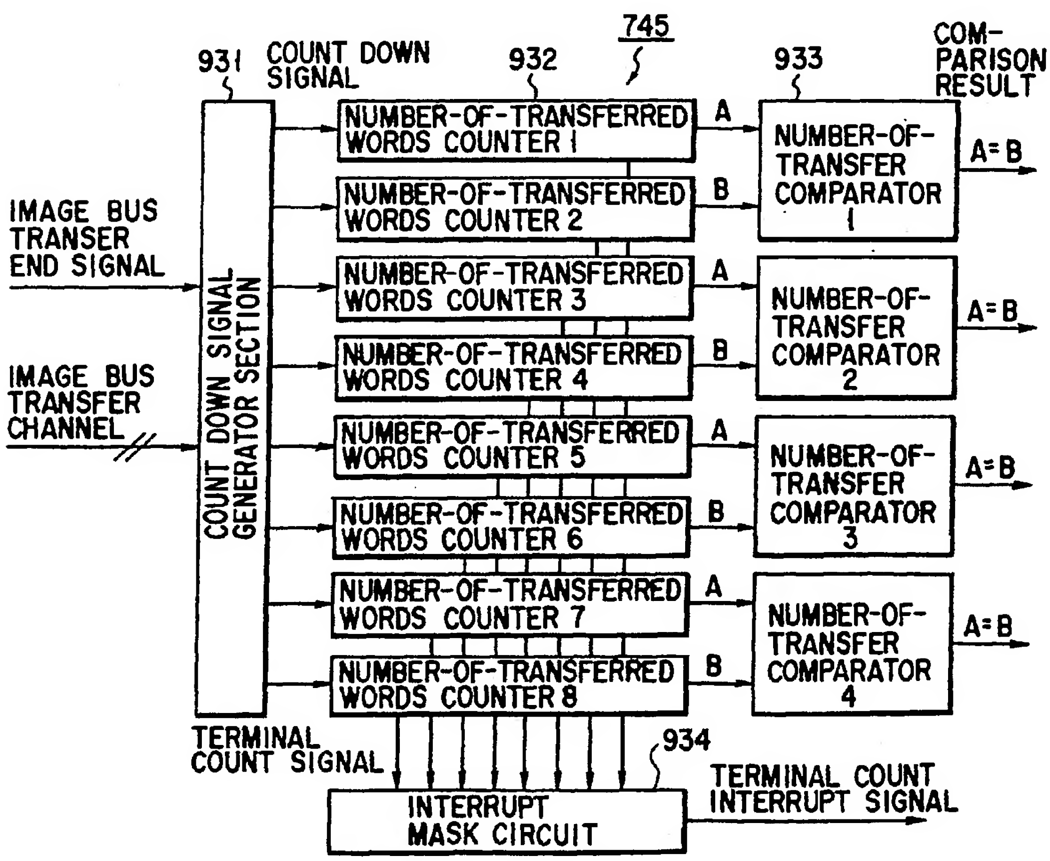
F I G. 17


741
910
911
912
IMAGE BUS
TRANSFER
REQUEST
MEDIATION
SECTION
REQUEST
MASK
CIRCUIT
REQUEST
GENERATOR
SECTION
CHANNEL 1
CHANNEL
BUFFER STATUS
(FOR 8 CHANNELS)
IMAGE BUS TRANSFER
REQUEST SIGNAL
(FOR 8 CHANNELS)
IMAGE BUS TRANSFER
ACKNOWLEDGE SIGNAL
(FOR 8 CHANNELS)
TC MASK
FIFO CONTROL MASK
TRANSFER
CHANNEL ENABL

F I G. 18


743
921
PAGE MEMORY TRANSFER REQUEST MEDIATION SECTION
922
REQUEST MASK CIRCUIT
923
REQUEST GENERATOR CHANNEL 1
CHANNEL BUFFER STATUS (FOR 8 CHANNELS)
TC MASK
FIFO CONTROL MASK
TRANSFER CHANNEL ENABLE
ADDRESS GENERATOR SELECT SIGNAL

F I G. 19


745
931
COUNT DOWN SIGNAL
932
933
COM-PARISON RESULT
IMAGE BUS TRANSER END SIGNAL
IMAGE BUS TRANSFER CHANNEL
COUNT DOWN SIGNAL GENERATOR SECTION
NUMBER-OF-TRANSFERRED WORDS COUNTER 1
NUMBER-OF-TRANSFERRED WORDS COUNTER 2
NUMBER-OF-TRANSFERRED WORDS COUNTER 3
NUMBER-OF-TRANSFERRED WORDS COUNTER 4
NUMBER-OF-TRANSFERRED WORDS COUNTER 5
NUMBER-OF-TRANSFERRED WORDS COUNTER 6
NUMBER-OF-TRANSFERRED WORDS COUNTER 7
NUMBER-OF-TRANSFERRED WORDS COUNTER 8
A
B
NUMBER-OF-TRANSFER COMPARATOR 1
NUMBER-OF-TRANSFER COMPARATOR 2
NUMBER-OF-TRANSFER COMPARATOR 3
NUMBER-OF-TRANSFER COMPARATOR 4
A=B
TERMINAL COUNT SIGNAL
934
INTERRUPT MASK CIRCUIT
TERMINAL COUNT INTERRUPT SIGNAL

F I G. 20

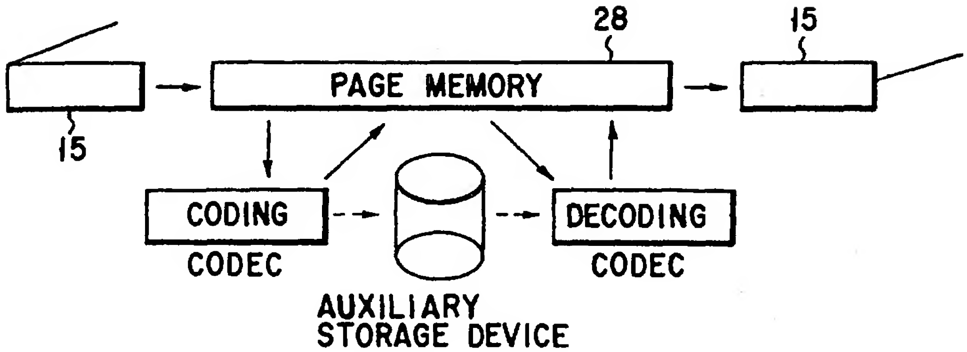

28
15
PAGE MEMORY
15
CODING
CODEC
DECODING
CODEC
AUXILIARY
STORAGE DEVICE

FIG. 21

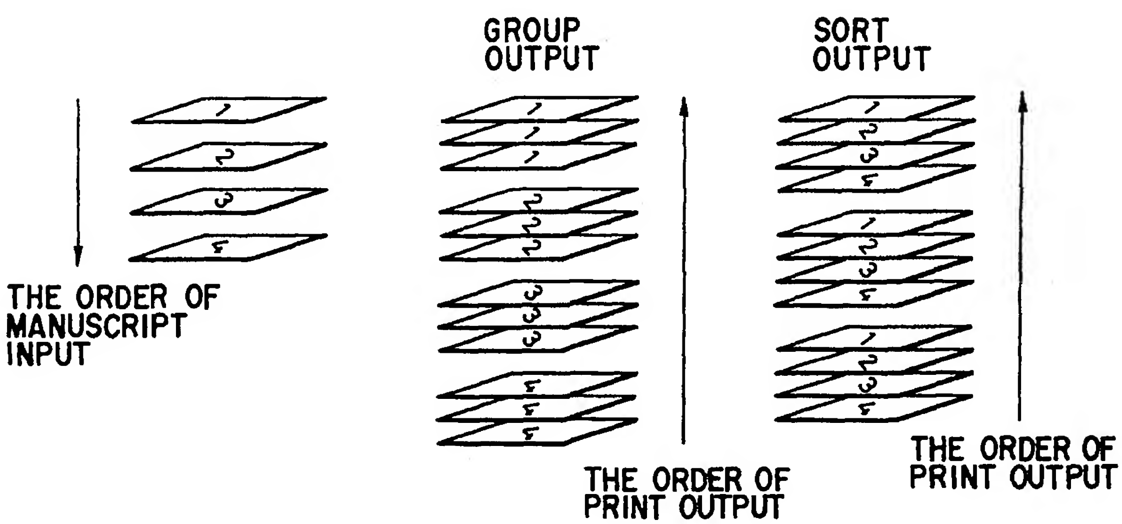

GROUP
OUTPUT
SORT
OUTPUT
THE ORDER OF
MANUSCRIPT
INPUT
THE ORDER OF
PRINT OUTPUT
THE ORDER OF
PRINT OUTPUT

FIG. 22

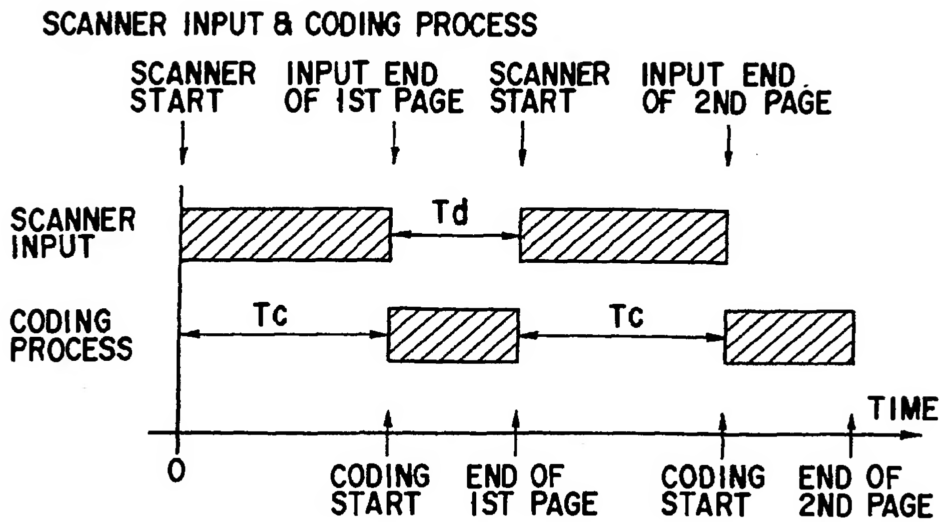


FIG. 23A
PRIOR ART

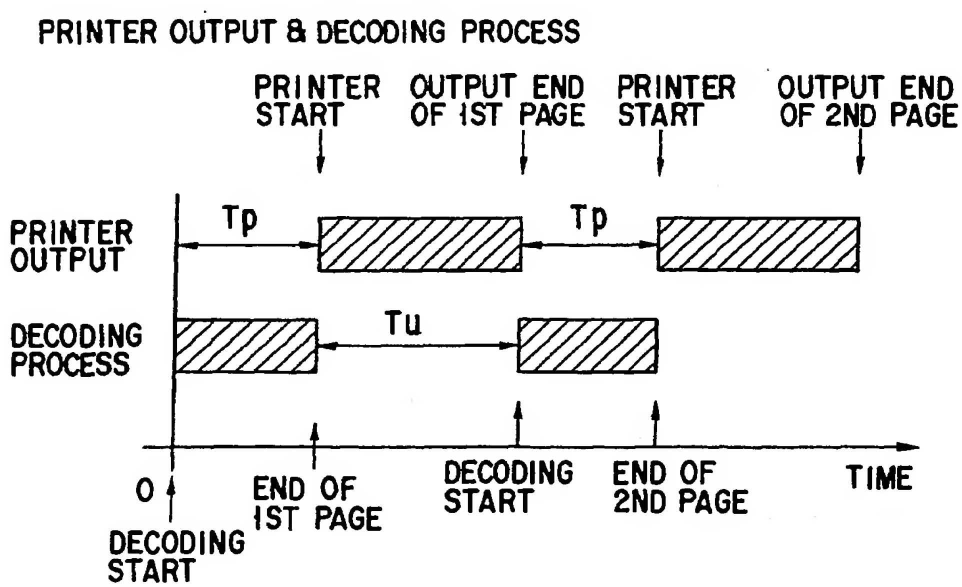
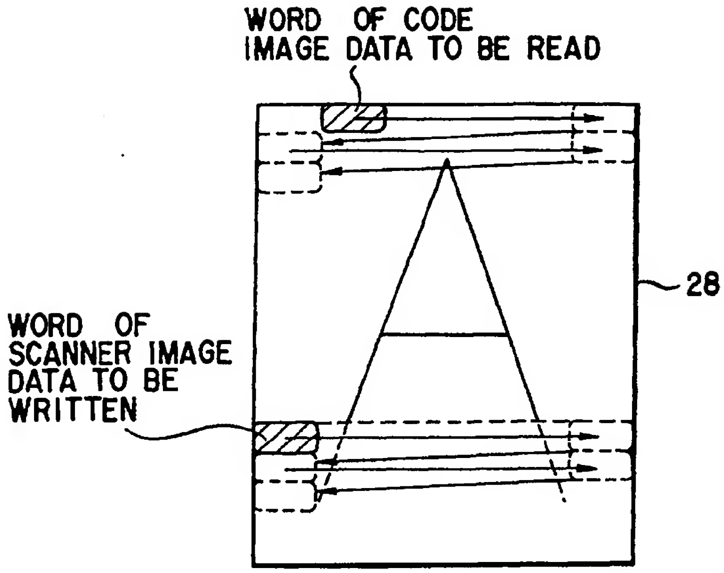
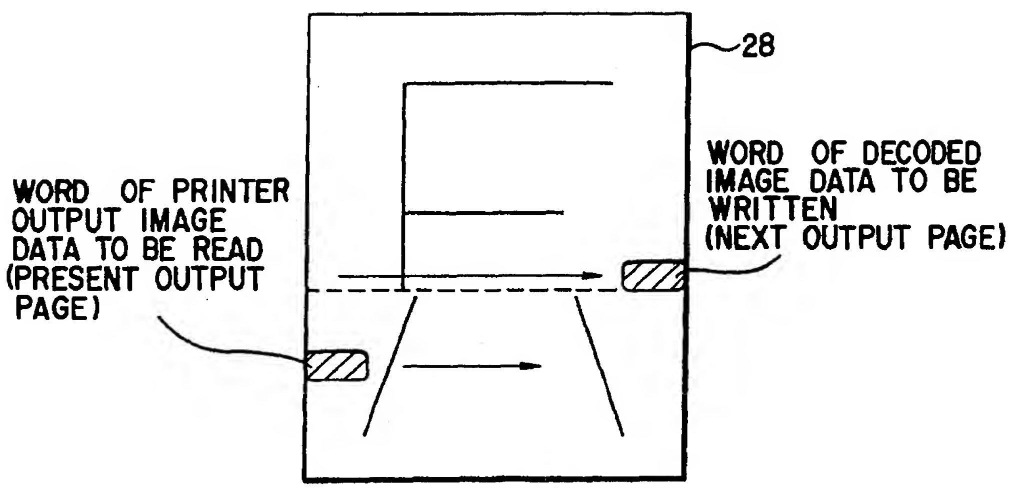


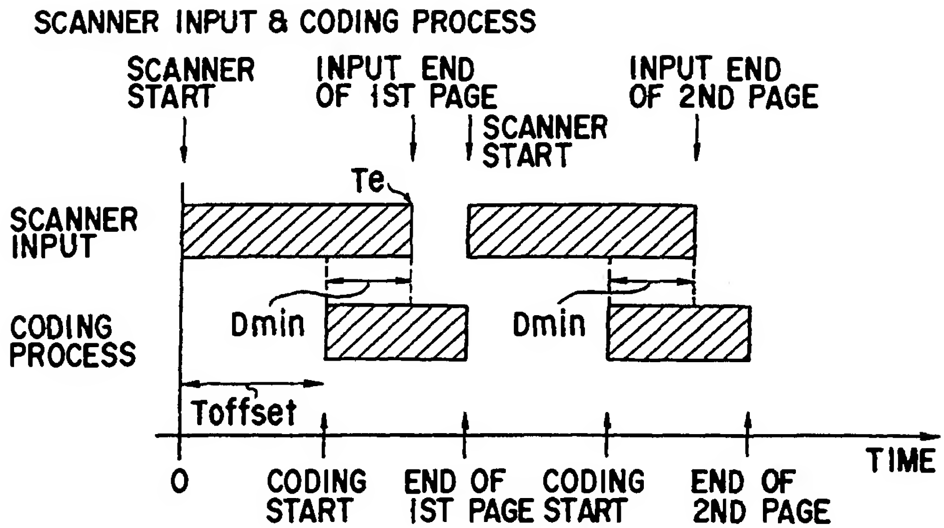
FIG. 23B
PRIOR ART



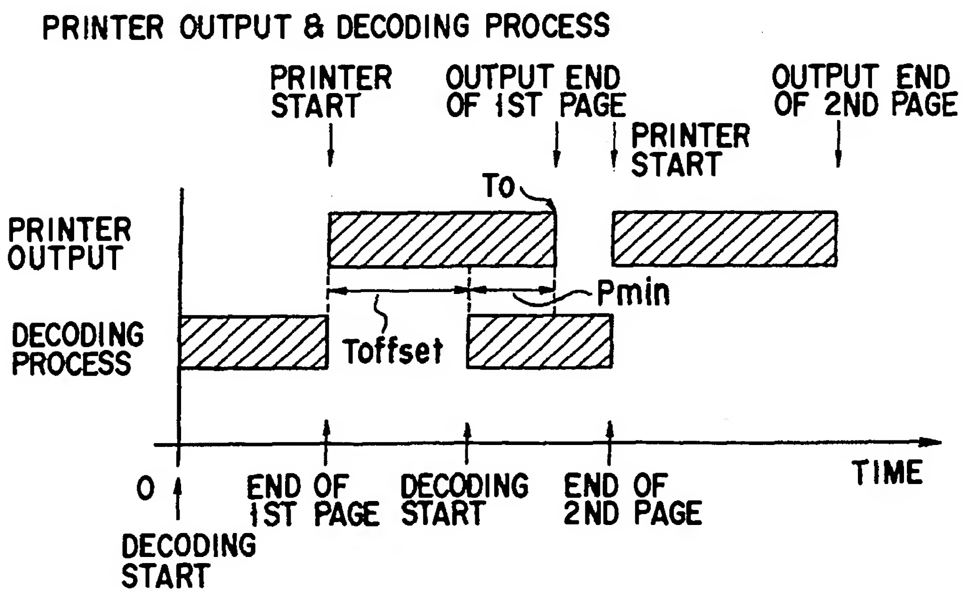
F I G. 24A



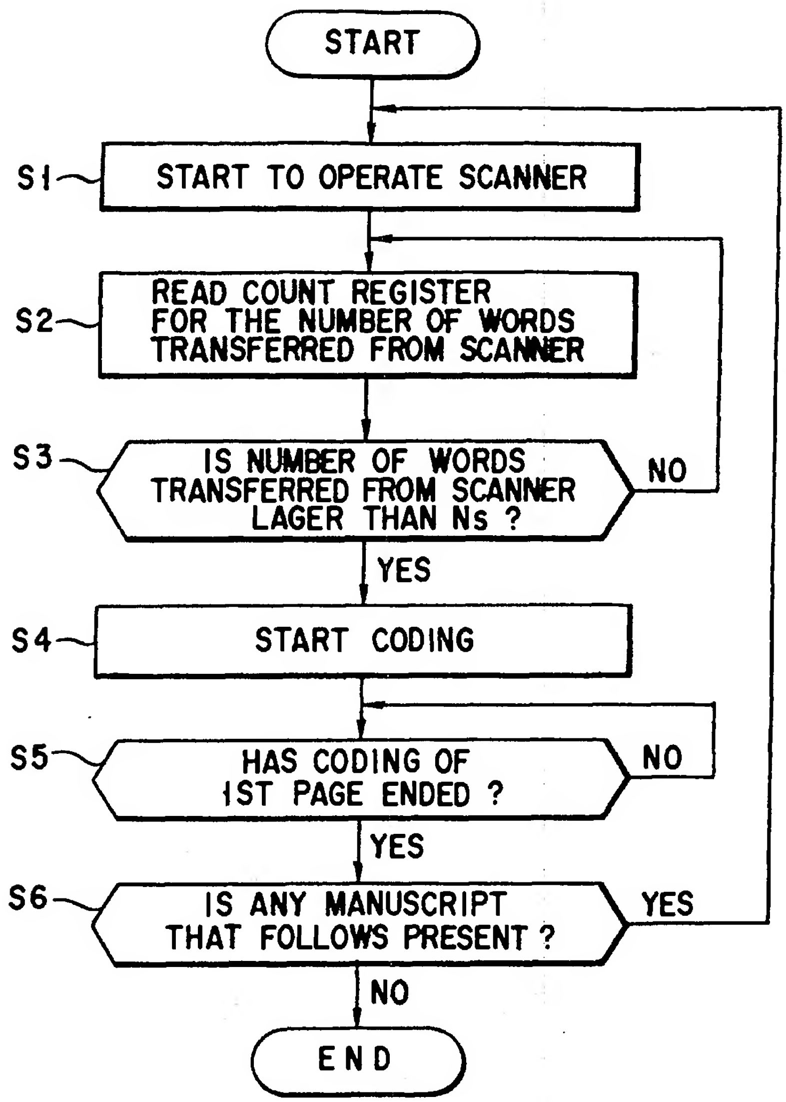
F I G. 24B



F I G. 25A



F I G. 25B


START
S1
START TO OPERATE SCANNER
S2
READ COUNT REGISTER FOR THE NUMBER OF WORDS TRANSFERRED FROM SCANNER
S3
IS NUMBER OF WORDS TRANSFERRED FROM SCANNER LAGER THAN Ns ?
NO
YES
S4
START CODING
S5
HAS CODING OF 1ST PAGE ENDED ?
NO
YES
S6
IS ANY MANUSCRIPT THAT FOLLOWS PRESENT ?
YES
NO
END

F I G. 26

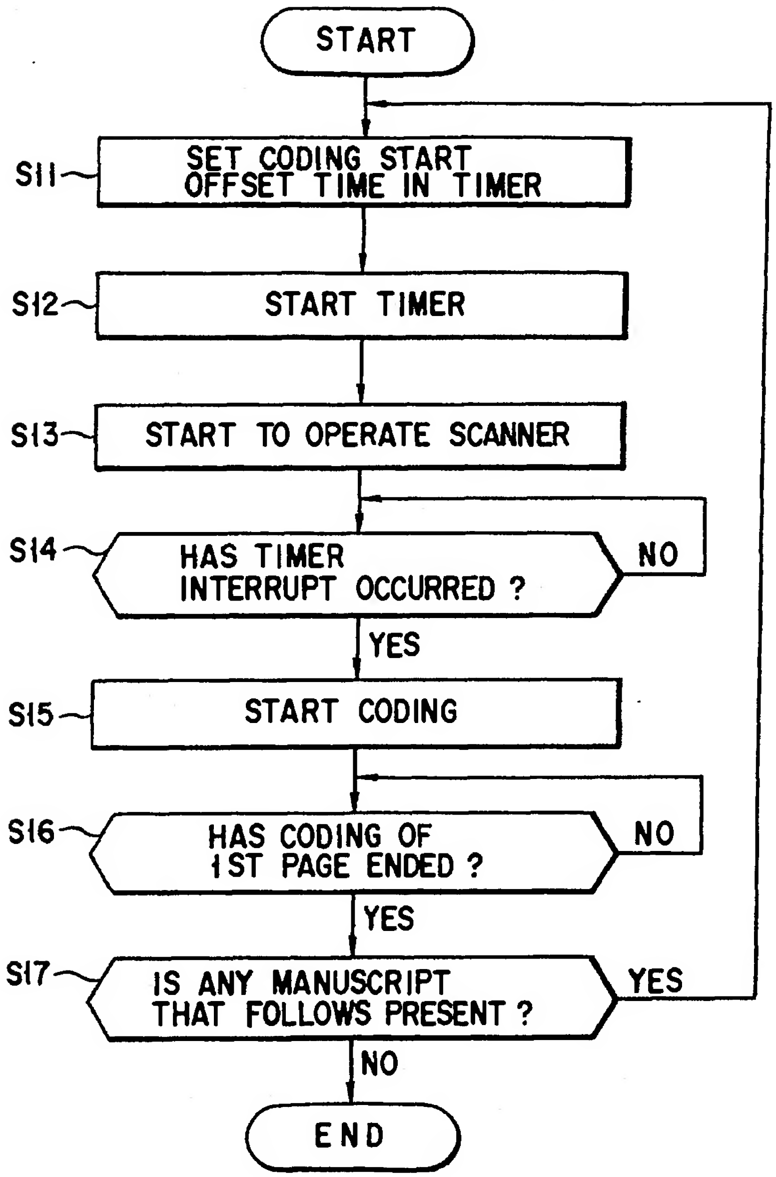

START
S11
SET CODING START OFFSET TIME IN TIMER
S12
START TIMER
S13
START TO OPERATE SCANNER
S14
HAS TIMER INTERRUPT OCCURRED ?
NO
YES
S15
START CODING
S16
HAS CODING OF 1ST PAGE ENDED ?
NO
YES
S17
IS ANY MANUSCRIPT THAT FOLLOWS PRESENT ?
YES
NO
END

FIG. 27

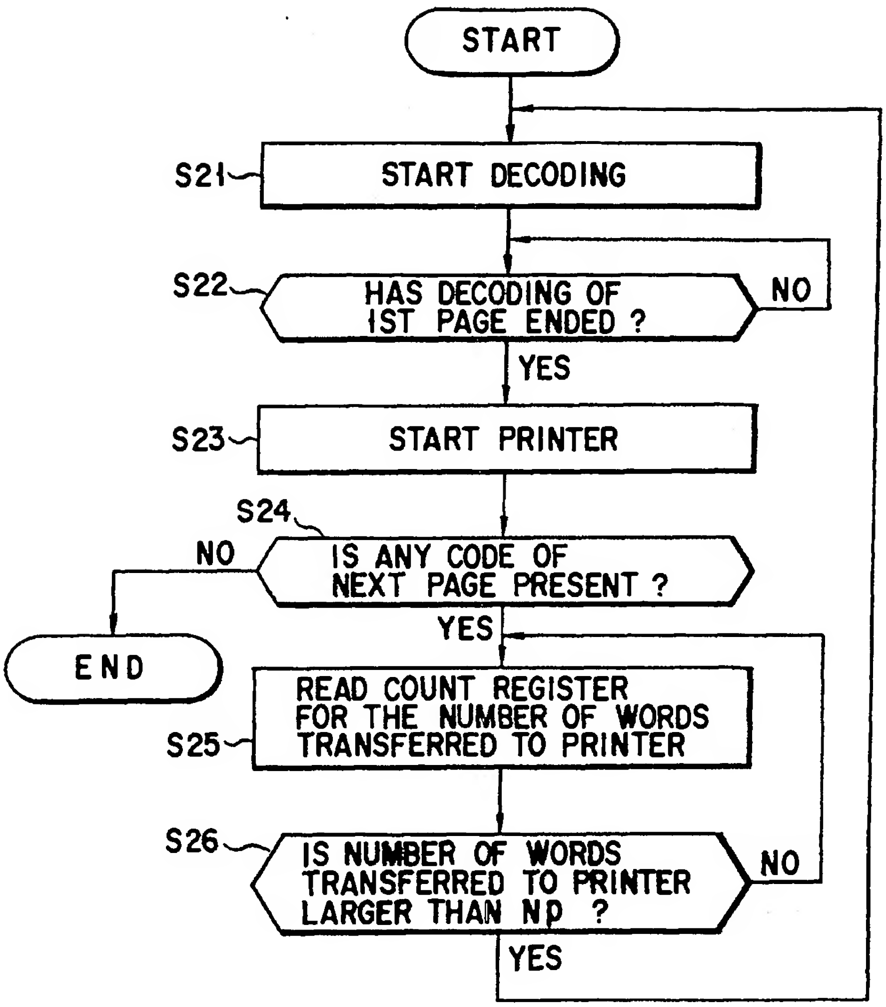

START
S21
START DECODING
S22
HAS DECODING OF
1ST PAGE ENDED ?
NO
YES
S23
START PRINTER
S24
NO
IS ANY CODE OF
NEXT PAGE PRESENT ?
YES
END
READ COUNT REGISTER
FOR THE NUMBER OF WORDS
TRANSFERRED TO PRINTER
S25
S26
IS NUMBER OF WORDS
TRANSFERRED TO PRINTER
LARGER THAN Np ?
NO
YES

FIG. 28

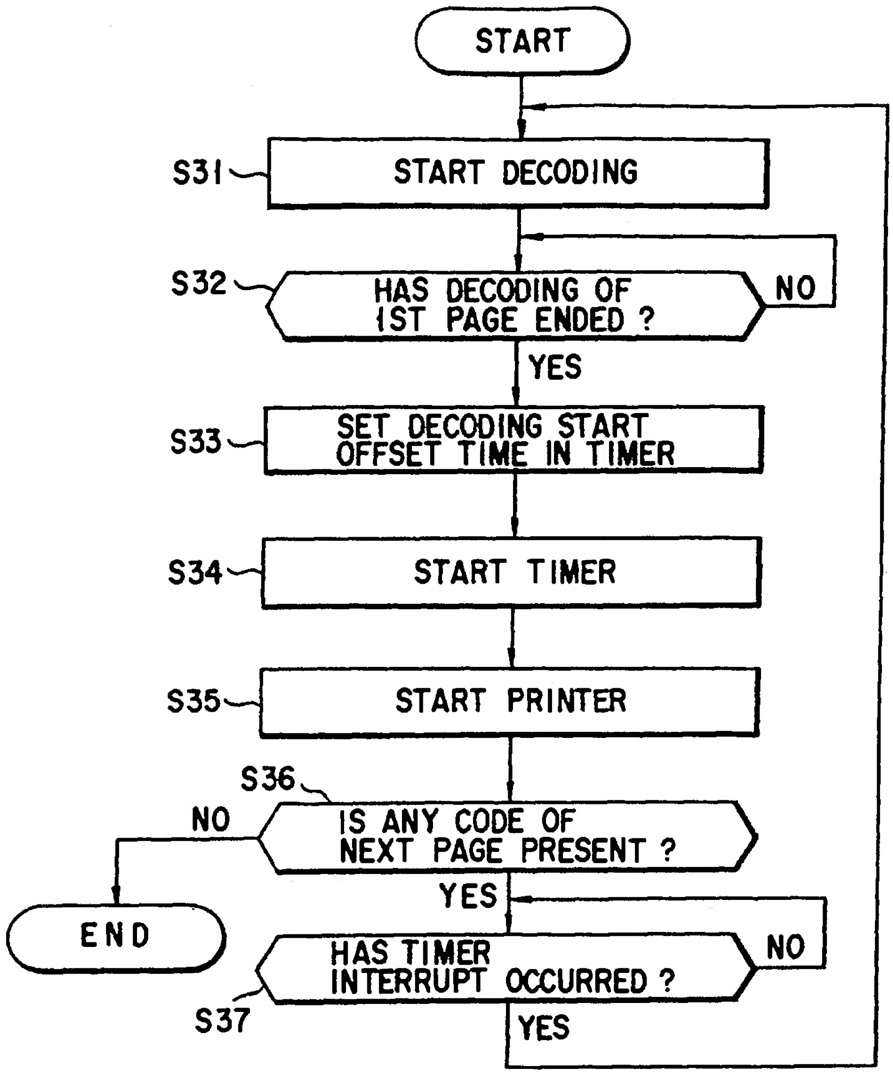
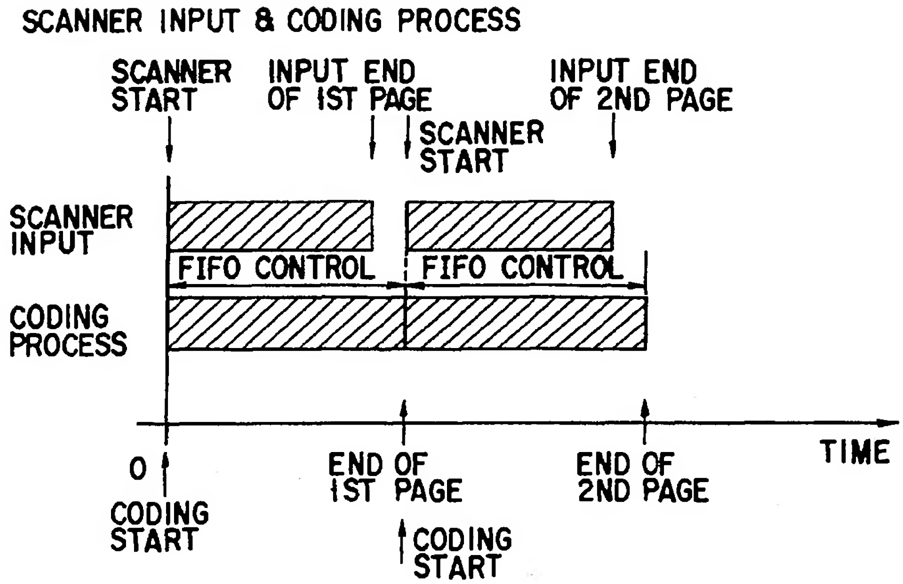
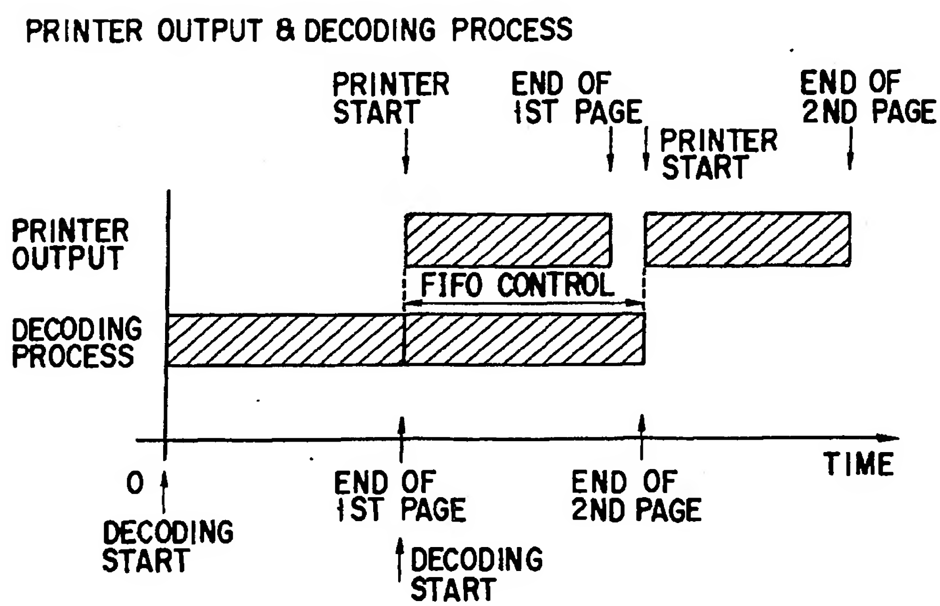

START
S31
START DECODING
S32
HAS DECODING OF
1ST PAGE ENDED ?
NO
YES
S33
SET DECODING START
OFFSET TIME IN TIMER
S34
START TIMER
S35
START PRINTER
S36
NO
IS ANY CODE OF
NEXT PAGE PRESENT ?
YES
END
HAS TIMER
INTERRUPT OCCURRED ?
NO
S37
YES

FIG. 29



F I G. 30A



F I G. 30B

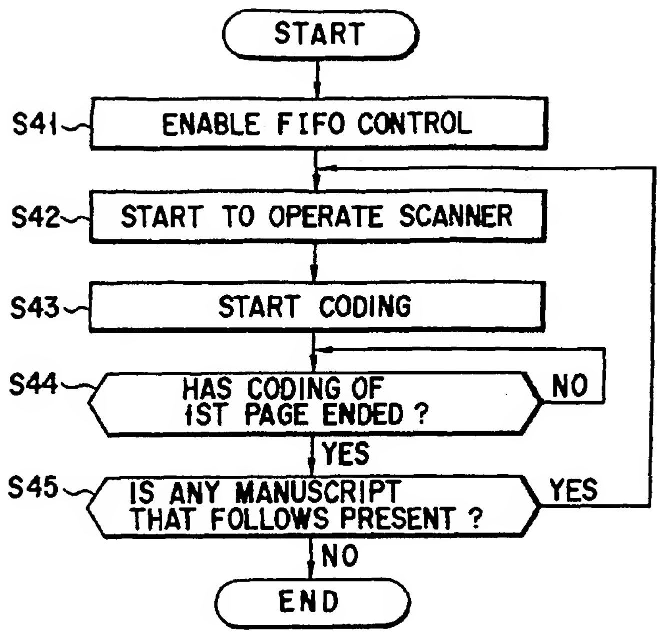

START
S41
ENABLE FIFO CONTROL
S42
START TO OPERATE SCANNER
S43
START CODING
S44
HAS CODING OF
1ST PAGE ENDED ?
NO
YES
S45
IS ANY MANUSCRIPT
THAT FOLLOWS PRESENT ?
YES
NO
END

FIG. 31

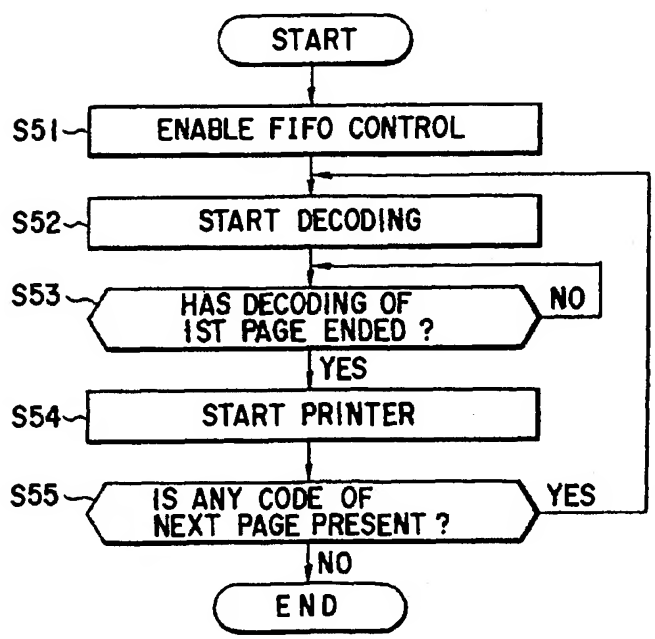
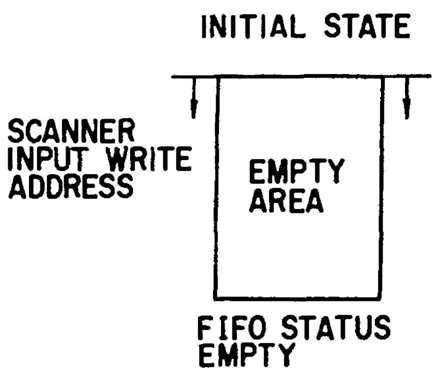
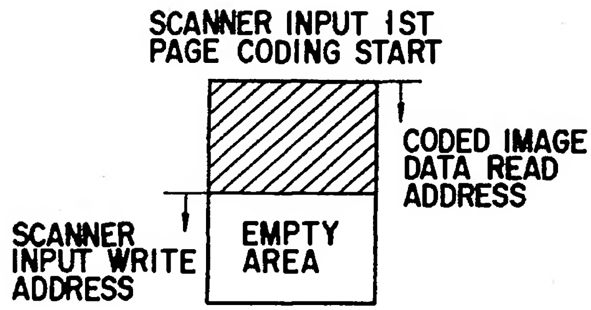

START
S51
ENABLE FIFO CONTROL
S52
START DECODING
S53
HAS DECODING OF
1ST PAGE ENDED ?
NO
YES
S54
START PRINTER
S55
IS ANY CODE OF
NEXT PAGE PRESENT ?
YES
NO
END

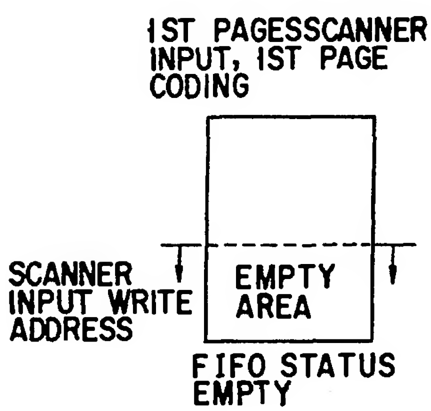
FIG. 32



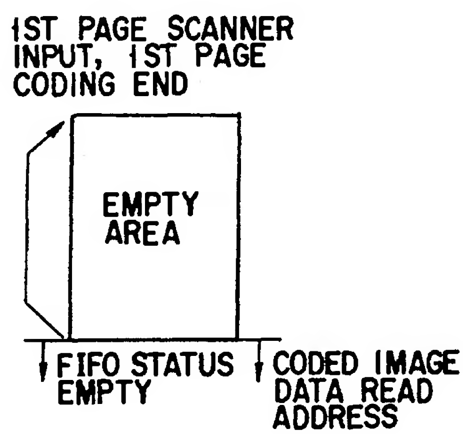
F I G. 33A



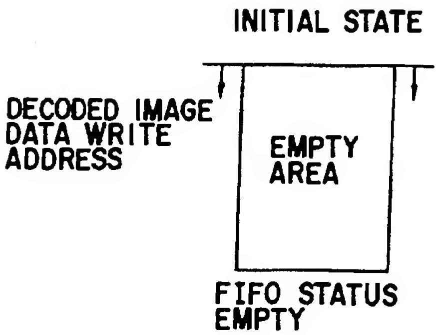
F I G. 33B



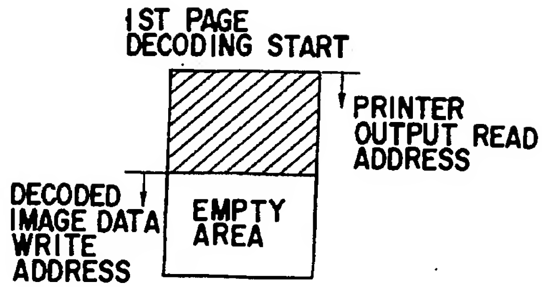
F I G. 33C



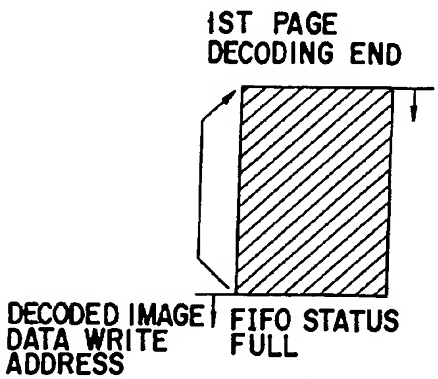
F I G. 33D



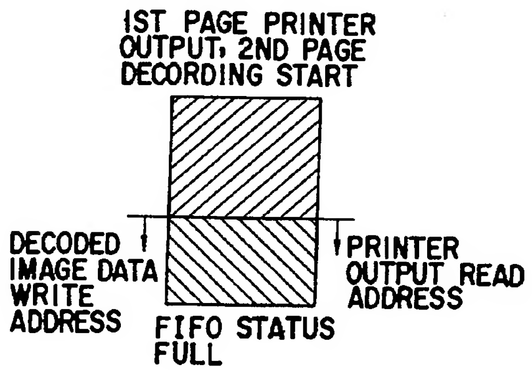
F I G. 34A



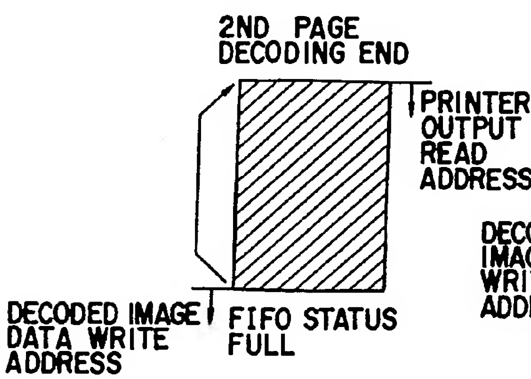
F I G. 34B



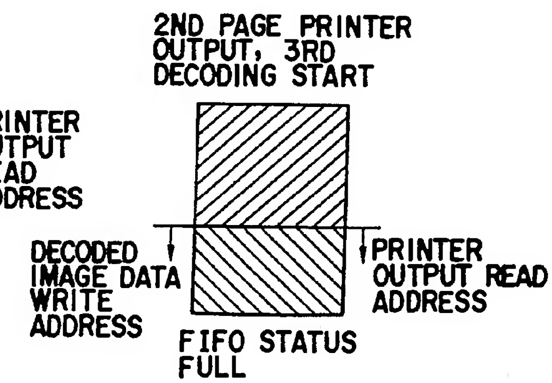
F I G. 34C



F I G. 34D



F I G. 34E



F I G. 34F